Dell/Compal LA-J143P

GDA30

Schematic Document

(Modena MLK Tiger Lake U)

Rev: 1.0(A00)

2020-07-14

Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

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Title: P001 - Cover		
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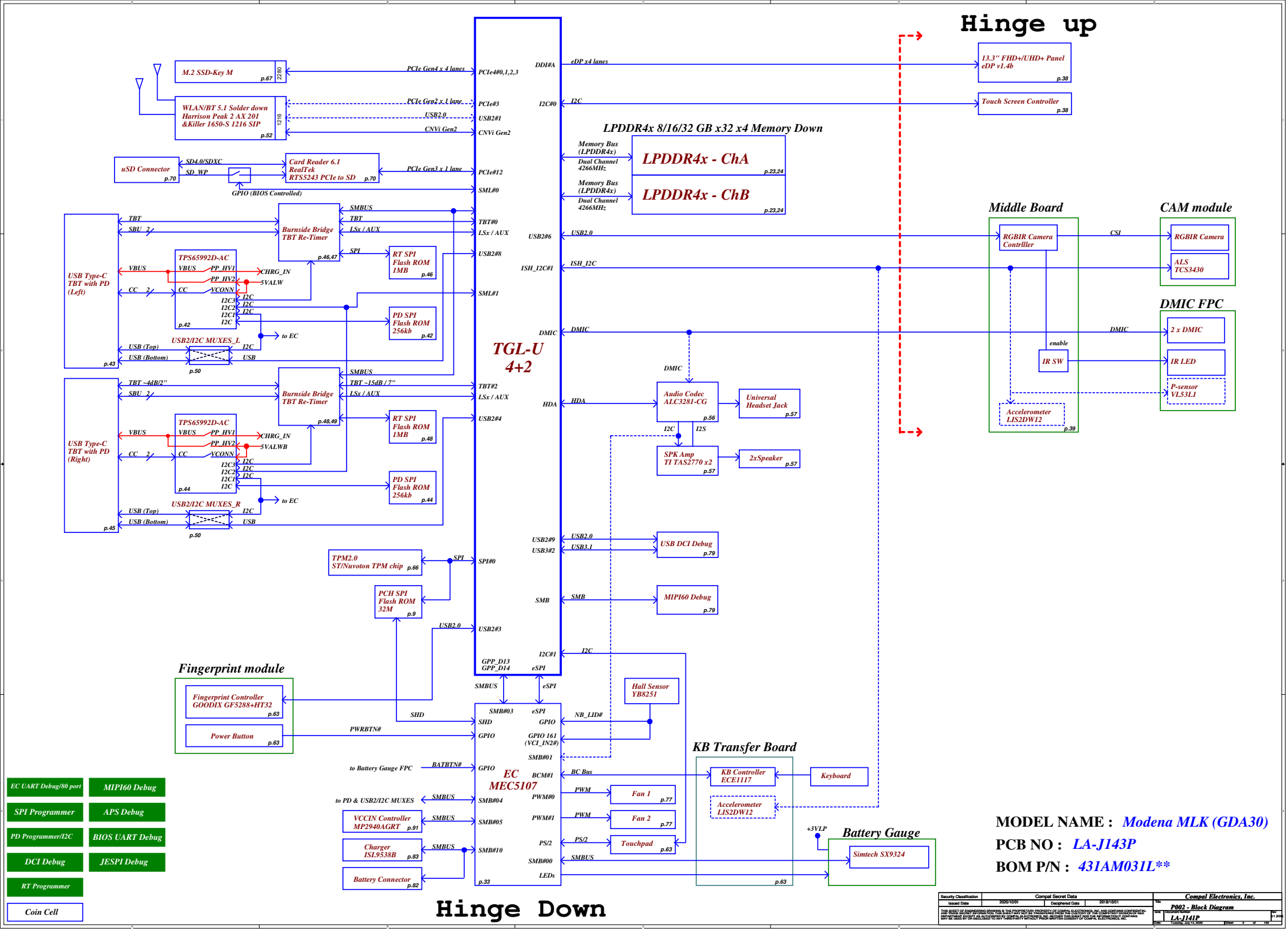
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MODEL NAME : Modena MLK (GDA30)
PCB NO : LA-J143P
BOM P/N : 431AM031L**
Hinge Down
Security Classification
Compal Secret Data
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2020/10/01
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2018/10/01
Compal Electronics, Inc.
P002 - Block Diagram
LA-J141P
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Board ID Table

Vcc	3.3V +/- 5%			
Board ID	R	C	REV	PCB Revision
0	240K +/- 1%	4700p	X00	0.1
1	130K +/- 5%	4700p	X01	0.2
2	62K +/- 5%	4700p	X02	0.3
3	33K +/- 5%	4700p		
4	8.2K +/- 5%	4700p		
5	4.3K +/- 5%	4700p	A00	1.0
6	2K +/- 5%	4700p		
7	1K +/- 5%	4700p	N/A	N/A

Board ID Option

RE194 X00@ 240K_0402_5% | RE194 X01@ 130K_0402_5% | RE194 X02@ 62K_0402_5% | RE194 X03@ 33K_0402_5% | RE194 X04@ 8.2K_0402_5% | RE194 A00@ 4.3K_0402_5%

SMBUS Control Table

	SOURCE	PCH	BATT Connector	Charger	IMVP9 Controller	PD Controller	MIPI60	USB/I2C MUX	BurnSide Bridge	TAP sensor	TI Amp.	Touch Pad	Touch Screen
SML0_SMBCLK SML0_SMBDATA	PCH								Reserve				
SML1_SMBCLK SML1_SMBDATA	PCH					V			V				
SMBCLK SMBDATA	PCH						V						
SML0B_SMBCLK SML0B_SMBDATA	PCH												
I2C_0_SCL I2C_0_SDA	PCH											V	
I2C_1_SCL I2C_1_SDA	PCH												V
EC_SMB00_CLK EC_SMB00_DAT	MEC5106									V			
EC_SMB01_CLK EC_SMB01_DAT	MEC5106										V		
EC_SMB02_CLK EC_SMB02_DAT	MEC5106											V	
EC_SMB03_CLK EC_SMB03_DAT	MEC5106	V											
EC_SMB04_CLK EC_SMB04_DAT	MEC5106					V		V					
EC_SMB05_CLK EC_SMB05_DAT	MEC5106				V								
EC_SMB10_CLK EC_SMB10_DAT	MEC5106		V	V									

Symbol Note :

@ : means de-pop

: means Digital Ground

: means Analog Ground

USB 2.0

USB 2.0 PORT#	DESTINATION
1	BT
2	None
3	FPR
4	Type-C_R
5	None
6	Camera
7	None
8	Type-C_L
9	USB DCI Debug
10	None

CLK

	DIFFERENTIAL	DESTINATION
CLK	CLKOUT_PCIE0	M.2 SSD Gen4
	CLKOUT_PCIE1	WLAN
	CLKOUT_PCIE2	None
	CLKOUT_PCIE3	None
	CLKOUT_PCIE4	Card Reader
	CLKOUT_PCIE5	None
	CLKOUT_PCIE6	None
	FLEX CLOCKS	DESTINATION
	ESPI_CLK	EC eSPI

Displayport

	DDI PORT#	DESTINATION
DDI	A	4 Lane eDP
	B	None

PCIE3/USB3.1

Flexible I/O	Interface	DESTINATION
1	PCI-E#1 / USB 3.1#1	WLAN PCIe Gen2
2	PCI-E#2 / USB 3.1#2	USB DCI Debug
3	PCI-E#3 / USB 3.1#3	None
4	PCI-E#4 / USB 3.1#4	None
5	PCI-E#5	None
6	PCI-E#6	
7	PCI-E#7	
8	PCI-E#8	
9	PCI-E#9	None
10	PCI-E#10	None
11	PCI-E#11 / SATA#0	None
12	PCI-E#12 / SATA#1a	Card Reader PCIE Gen2

PCIE4

Flexible I/O	Interface	DESTINATION
0	PCIE4 #0	M.2 SSD PCIE Gen4
1	PCIE4 #1	
2	PCIE4 #2	
3	PCIE4 #3	

Thunderbolt

	TBT PORT#	DESTINATION
TBT	0	USB Type-C_L
	1	None
	2	USB Type-C_R
	3	None

X76 — DRAM Option R1

X7682731L55	Micron 8GB/4266
X7682731L56	Micron 16GB/4266
X7682731L58	Micron 32GB/4266
X7682731L59	Hynix 8GB/4266
X7682731L52	Hynix 16GB/4266
X7682731L62	Hynix 32GB/4266
X7682731L60	Samsung 8GB/4266
X7682731L57	Samsung 16GB/4266
X7682731L53	Samsung 32GB/4266
X7682731L54	Micron 4GB/4266
X7682731L51	Hynix 4GB/4266
X7682731L61	Samsung 4GB/4266

DRAM Config Option (Resistor pop location)

MEM_CONFIG0 | MEM_CONFIG1 | MEM_CONFIG2 | MEM_CONFIG3 | MEM_CONFIG4

EVT1_4

EVT1_3T

CPU ID Option

RE539 NVPRO_I5@ 63K_0402_5% | RE539 NVPRO_I7@ 33K_0402_5% | RE539 VPRO_I5@ 240K_0402_5% | RE539 VPRO_I7@ 130K_0402_5% | RE539 C3@ 8.2K_0402_5%

PCB

ZZ FIT@ LA-J142P | ZZ PCB@ LA-J143P

EVT1_5

CPU Option

UC1 NVPRO_I5@ SA0000DTU2L SRK05 | UC1 NVPRO_I7@ SA0000DT2L SRK02 | UC1 VPRO_I5@ SA0000DRH1L QVBC | UC1 VPRO_I7@ SA0000DRT1L QVB6 | UC1 C3@ SA0000DTV2L SRK0B

TBT Option

UIT1 BB@ SA0000CAH3L JHL8040R QURW | UIT2 BB@ SA0000CAH5L JHL8040R QURW

PD Option

UPD1 PD_AC@ SA0000DLV00 PTPS65992DAC | UPD2 PD_AC@ SA0000DLV00 PTPS65992DAC | UPD1 PD_AD@ SA0000D9100 PTPS65992DAD | UPD2 PD_AD@ SA0000D9100 PTPS65992DAD

WLAN Option

UWL1 CNV@ PK29500L1L KILLER1650S.04 | UWL1 DAR@ PK29500B62L WBQ76QOUS01

TPM Option

UT12 ST_AHC1@ SA0000C5G10 ST33HTPH2032AHC1 | UT12 ST_AHC4@ SA0000CY000 ST33HTPH2X32AHC4 | UT12 ST_AHD4@ SA0000CY010 ST33HTPH2X32AHD4

EC Option

UE1 NPI_5107@ SA0000CQ730 MEC5107K-D4-LJ-TR ES | UE1 MP_5107@ SA0000CQ740 MEC5107K-D4-LJ-TR NON-ES

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Title: P003 - Notes List

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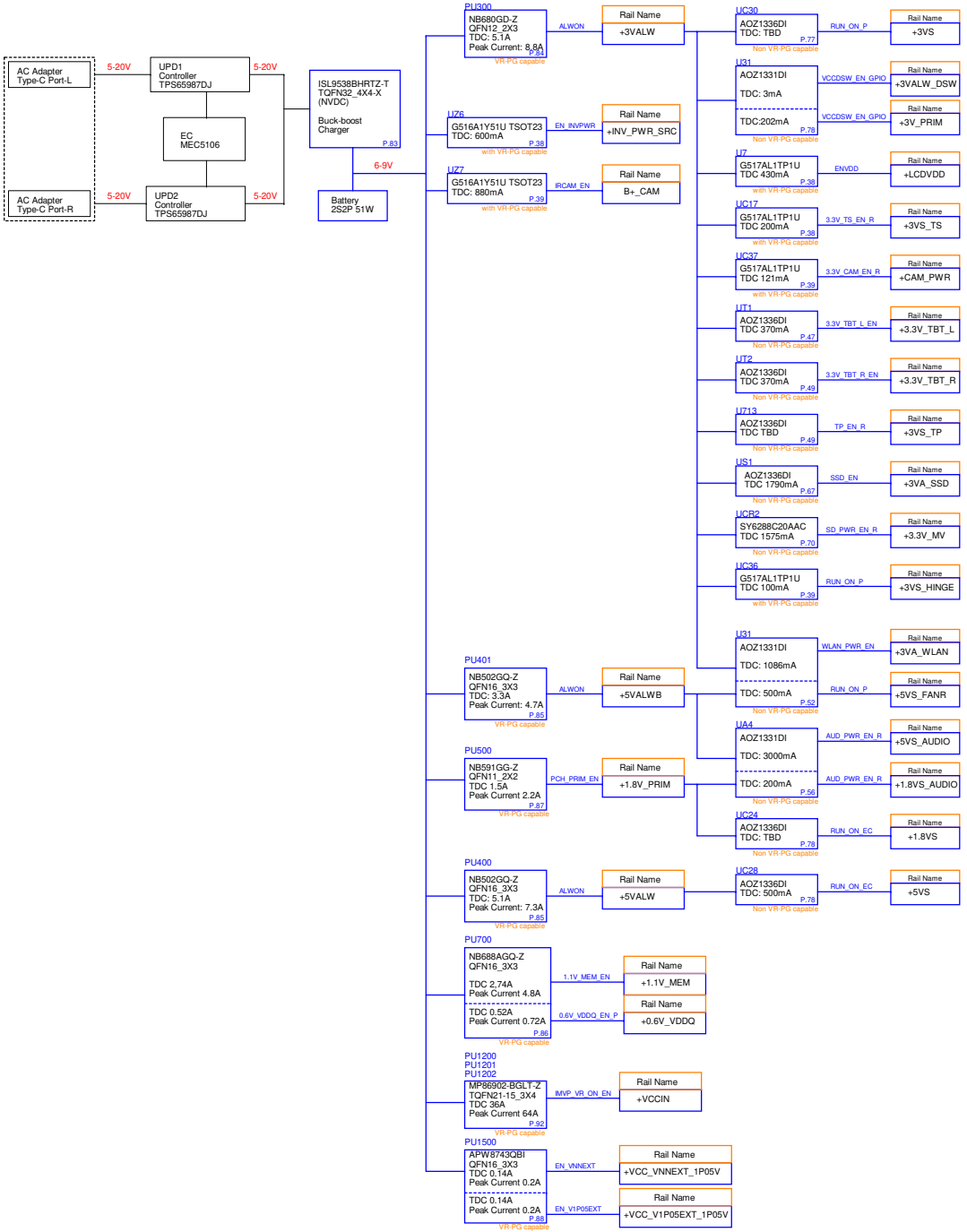
Date: Tuesday, August 11, 2020 | Sheet 3 of 109



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Issued Date	2017/08/24	Deciphered Date 2017/08/24	Title: P004 - Power MAP

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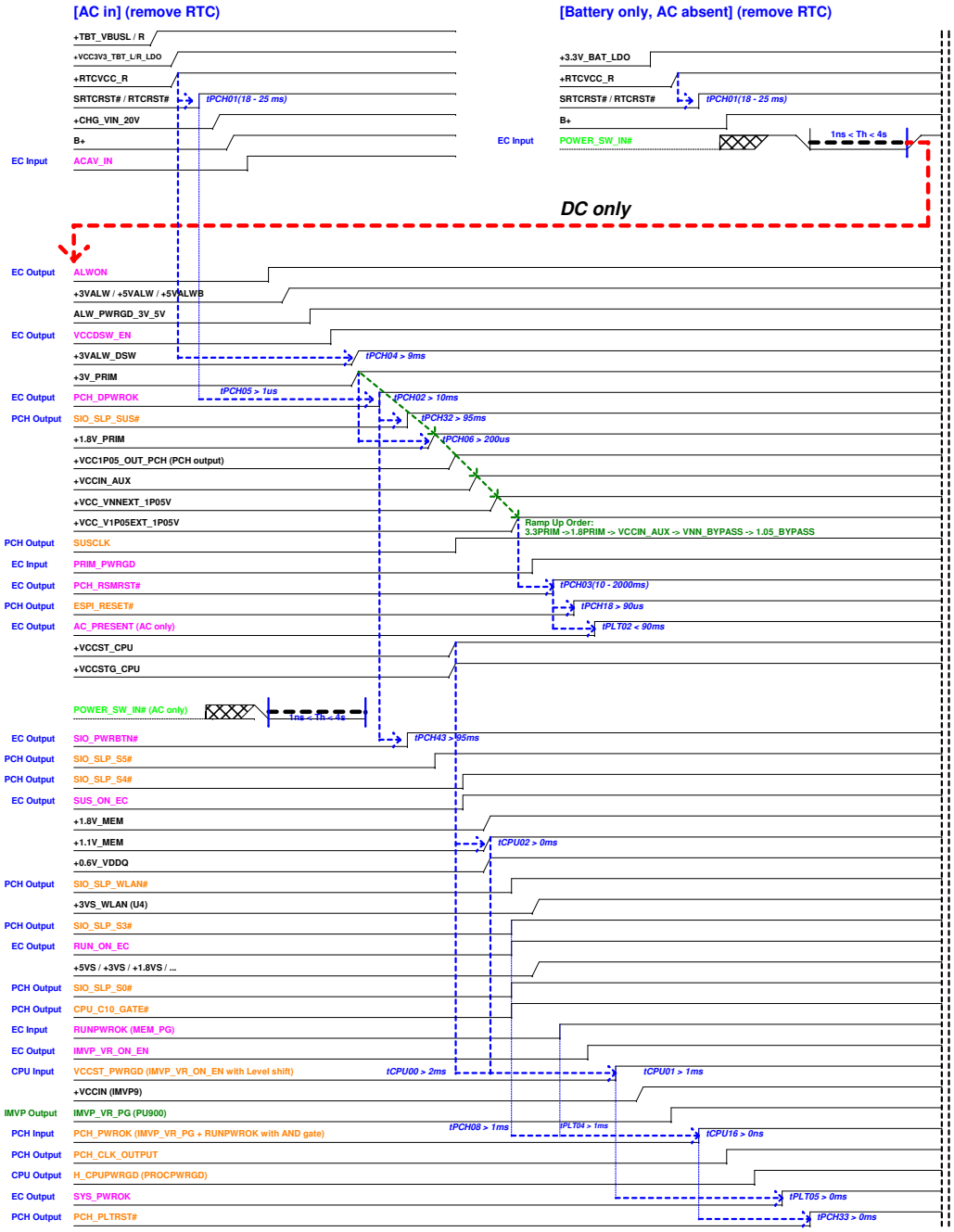
Size	Document Number	Rev
	LA-G172P	0.6
Date: Tuesday, July 04, 2017	Sheet 4 of 39	

Power Sequence
G3 -> S0



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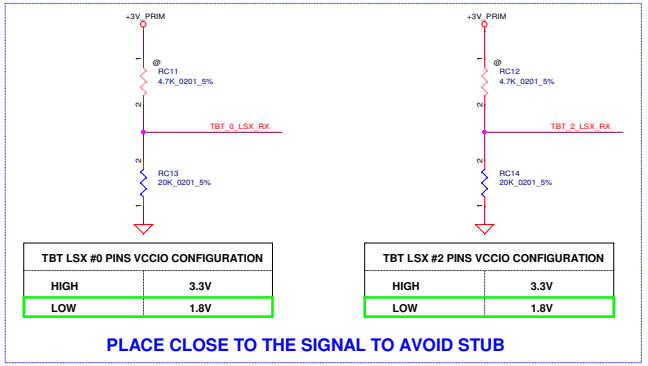
Title	P005 - Power Sequence		
Size	Document Number		Rev
	LA-J141P		1.1 (0G)
Date:	Tuesday, July 14, 2020	Sheet 5 of 100	



TBT LSX #0 PINS VCCIO CONFIGURATION	
HIGH	3.3V
LOW	1.8V

TBT LSX #2 PINS VCCIO CONFIGURATION	
HIGH	3.3V
LOW	1.8V

PLACE CLOSE TO THE SIGNAL TO AVOID STUB

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Title	P006 - TGL-U(1/13)TCSS,EDP
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Date:	Tuesday, July 14, 2020
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DIMM TYPE	BOOT STRAP 3	BOOT STRAP 2	BOOT STRAP 1	Reserved	Reserved
1 : Interleave 0 : Non-Interleave	GPP_H2 (Weak internal PD 20K) This is bit 3 of a total of 4-bit encoded pin straps for boot configuration.	GPP_H1 (Weak internal PD 20K) This is bit 2 of a total of 4-bit encoded pin straps for boot configuration.	GPP_H0 (Weak internal PD 20K) This is bit 1 of a total of 4-bit encoded pin straps for boot configuration.	GPP_F7 (Weak internal PD 20K)	GPP_F10 (Weak internal PD 20K)

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Compal Electronics, Inc.	
Title	P007 - TGL-U(2/13)MISC,MIPI60
Size	Document Number: LA-J141P
Rev	0.1 (X00)
Date:	Tuesday, July 14, 2020
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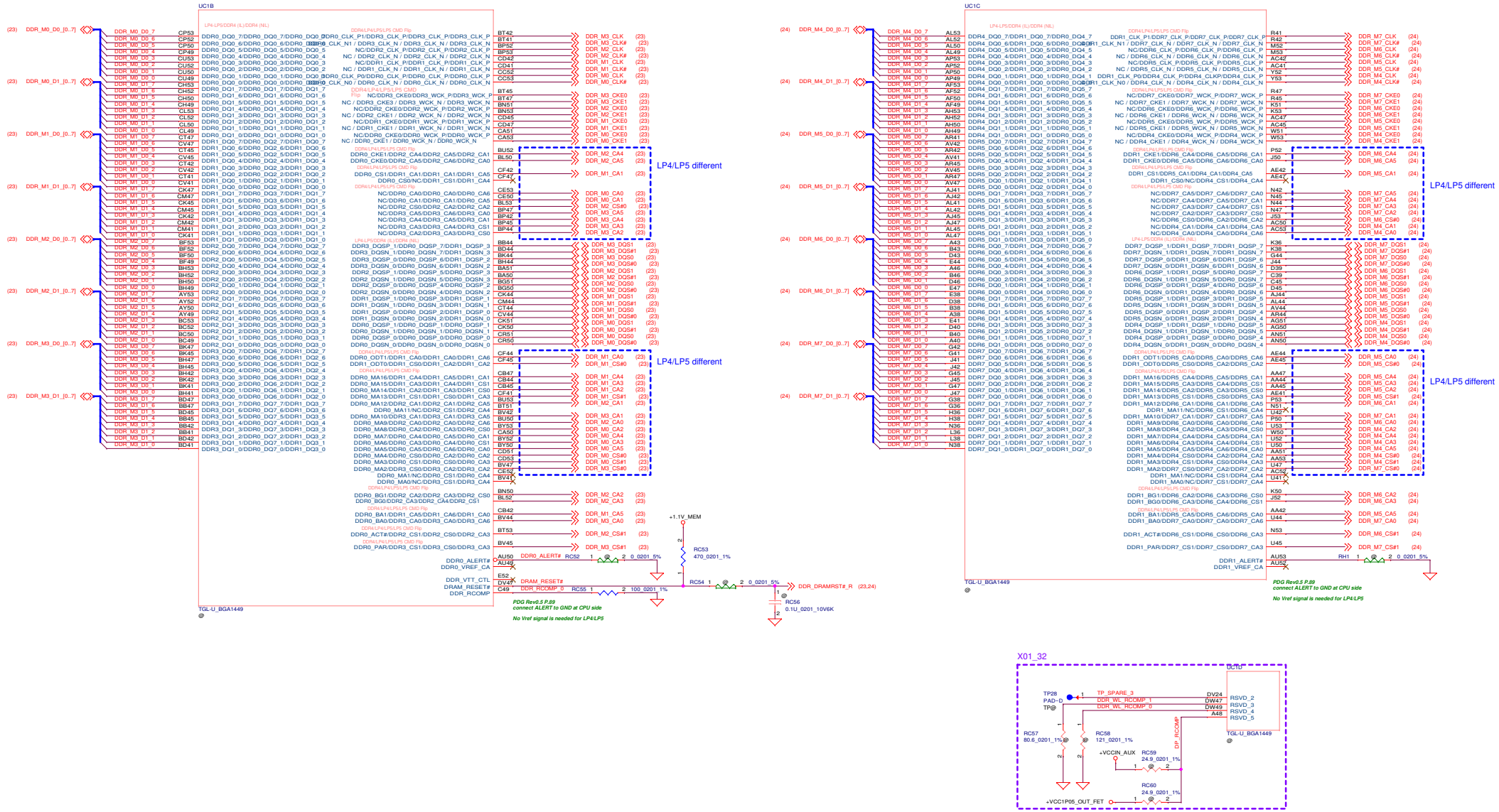

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Title: **P008 - TGL-U(3/13)LPDDR4/x**

Size: — Document Number: **LA-J141P** — Rev: 0.1 (X00)

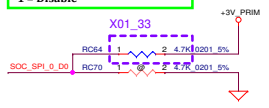
Date: Tuesday, July 14, 2020 — Sheet 8 of 100

BOOT HALT

SPI0_MOSI(NO INTERNAL PU/PD)

0 = Enable

1 = Disable

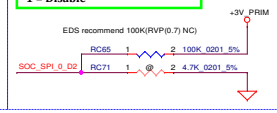


CONSENT STRAP

SPI0_IO2(NO INTERNAL PU/PD)

0 = Enable

1 = Disable

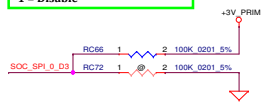


A0 PERSONALITY STRAP

SPI0_IO3

0 = Enable

1 = Disable

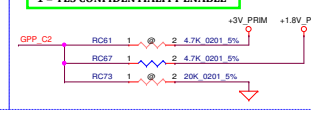


TLS CONFIDENTIALITY

GPP_C2 (Weak internal PD 20K)

0 = TLS CONFIDENTIALITY DISABLE

1 = TLS CONFIDENTIALITY ENABLE

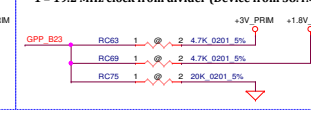


CPUNSSC CLOCK FREQ

GPP_B23 (Weak internal PD 20K)

0 = 38.4 MHz clock direct from crystal (default)

1 = 19.2 MHz clock from divider (Device from 38.4MHz crystal)

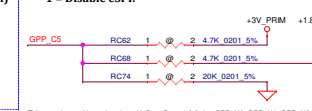


ESPI OR EC LESS

GPP_C5 (Weak internal PD 20K)

0 = Enable eSPI. (Default)

1 = Disable eSPI.



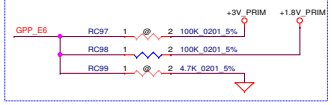
This strap is used in conjunction with Boot Strap 1,2,3, (on GPP_H0, GPP_H1, GPP_H2 respectively).

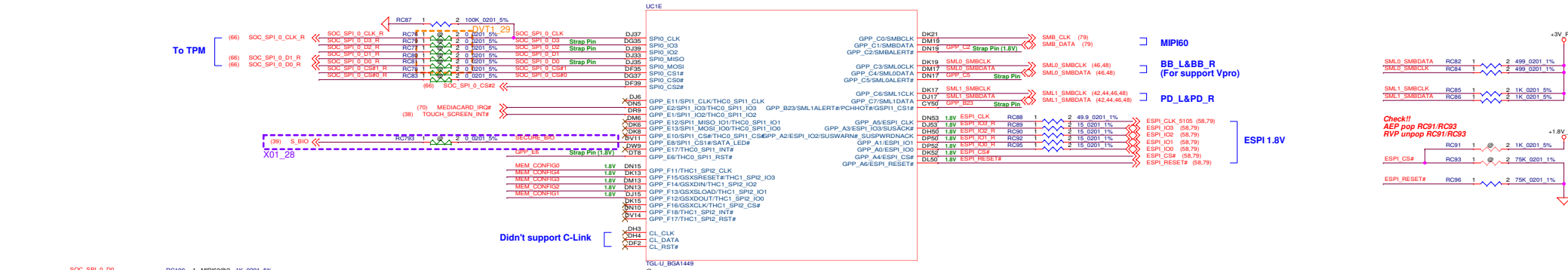
0000 = Master Attached Flash Configuration (BIOS / CSME on SPI). <--use this

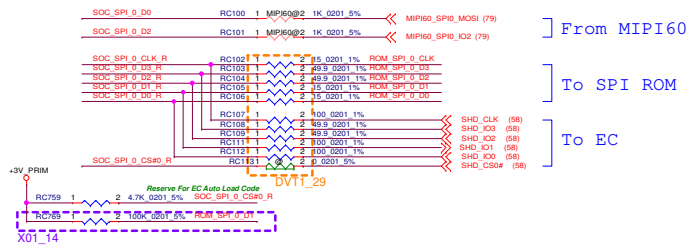
1000 = Slave Attached Flash Configuration (BIOS / CSME on eSPI attached device).
0100 = BIOS on eSPI Peripheral Channel; CSME on master attached SPI.
1100 = BIOS on eSPI peripheral Channel; CSME on slave attached SPI.
Others: Reserved.

Reserved

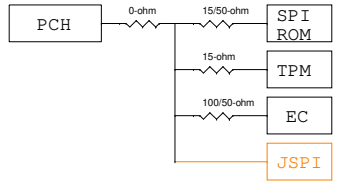
GPP_E6 (External pull-up is required)



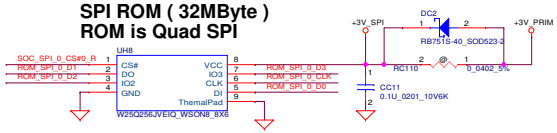


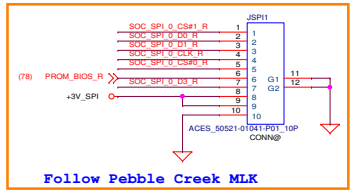


SPI0 EC G3 Flash Sharing Topology
Ref 607872_TGL_UP3_PDG_Rev1p1
2-Load Branch Topology (Device Down) with EC Wired-OR Flash Sharing and TPM

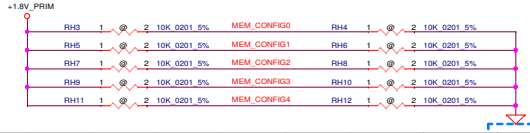


SPI ROM (32MByte)
ROM is Quad SPI





Memory Type Configuration Strap pin



Pin Name	Micron 8GB SA0000BX50L	Micron 16GB SA0000BX60L	Micron 32GB SA0000BX70L	Hynix 8GB SA0000BYX0L	Hynix 16GB SA0000BY90L	Hynix 32GB SA0000BW00L	Samsung 8GB SA0000C60L0	Samsung 16GB SA0000C6L0L	Samsung 32GB SA0000CGN0L	Micron 4GB SA0000BX50L	Hynix 4GB SA0000BYX0L	Samsung 4GB SA0000C6K0L
MEM_CONFIG0	0	1	0	1	0	1	0	1	0	0	1	0
MEM_CONFIG1	0	0	1	1	1	0	1	0	0	0	1	1
MEM_CONFIG2	0	0	0	0	0	1	1	0	0	0	0	1
MEM_CONFIG3	0	0	0	0	1	0	0	1	1	0	0	0
MEM_CONFIG4	0	0	0	0	0	0	0	0	0	1	1	1

EV11_31

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Title	P009 - TGL-U(4/13)SPI,SMB,ESPI
Size	Document Number: LA-J141P
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Date:	Tuesday, July 14, 2020
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TOP SWAP OVERRIDE

GPP_B14 / SPKR (Internal 20 K Pull Down)

0 = Disable "Top Swap" mode. (Default)

1 = Enable "Top Swap" mode.

NO REBOOT

GPP_B18/GSPI0_MOS (Internal 20 K Pull Down)

0 = REBOOT ENABLED

1 = NO REBOOT (This function is useful when running ITP/XDP).

FLASH DESCRIPTOR SECURITY OVERRIDE

GPP_R2/HDA_SDO (Internal 20 K Pull Down)

0 = ENABLE (DEFAULT)

1 = DISABLE (ME can update)

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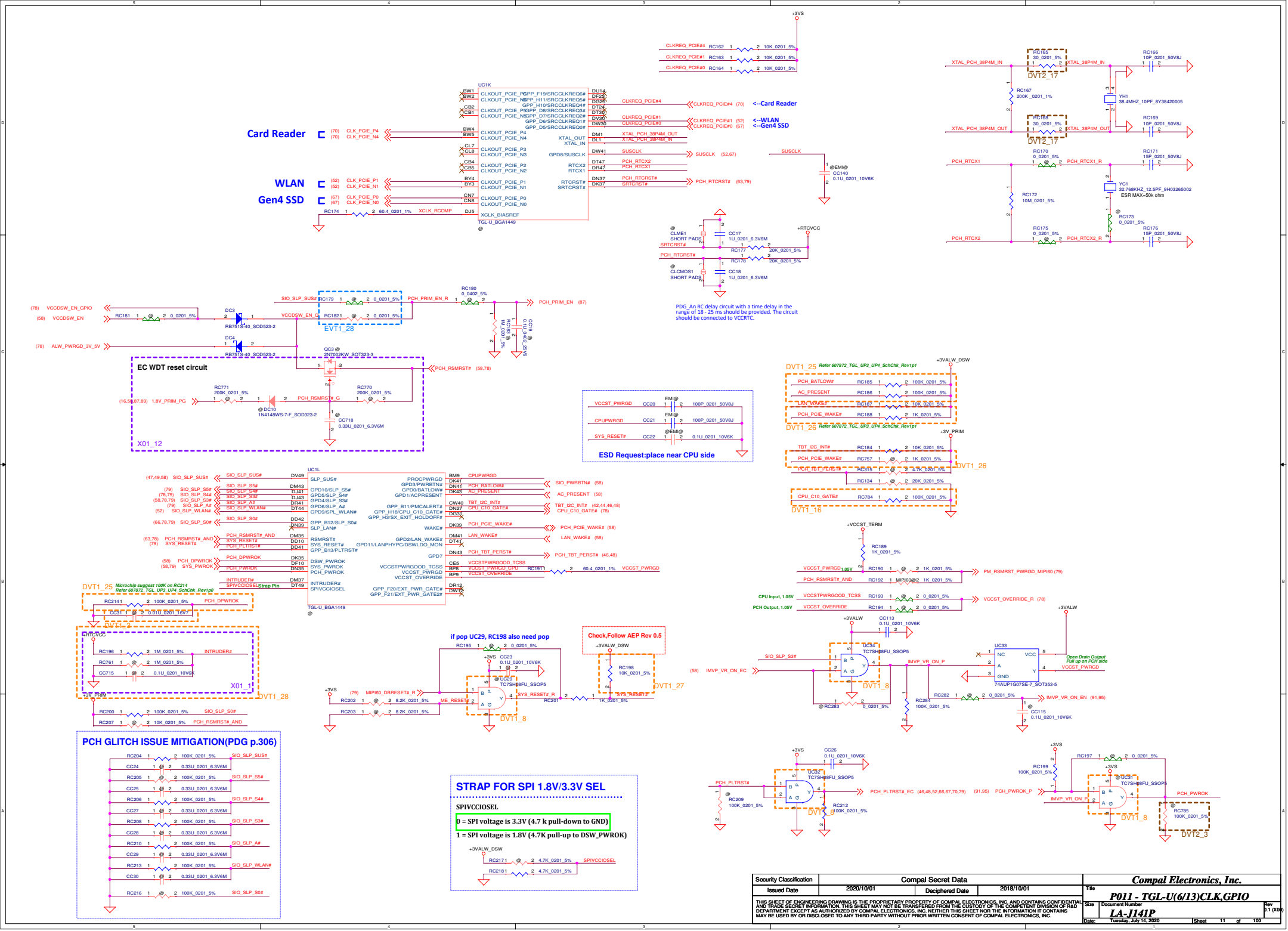
Compal Electronics, Inc.	
Title	P010 - TGL-U(5/13)HDA,I2C,ISH
Size	Document Number: LA-J141P
Rev	0.1 (X00)
Date:	Thursday, July 30, 2020
Sheet	10 of 100



Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

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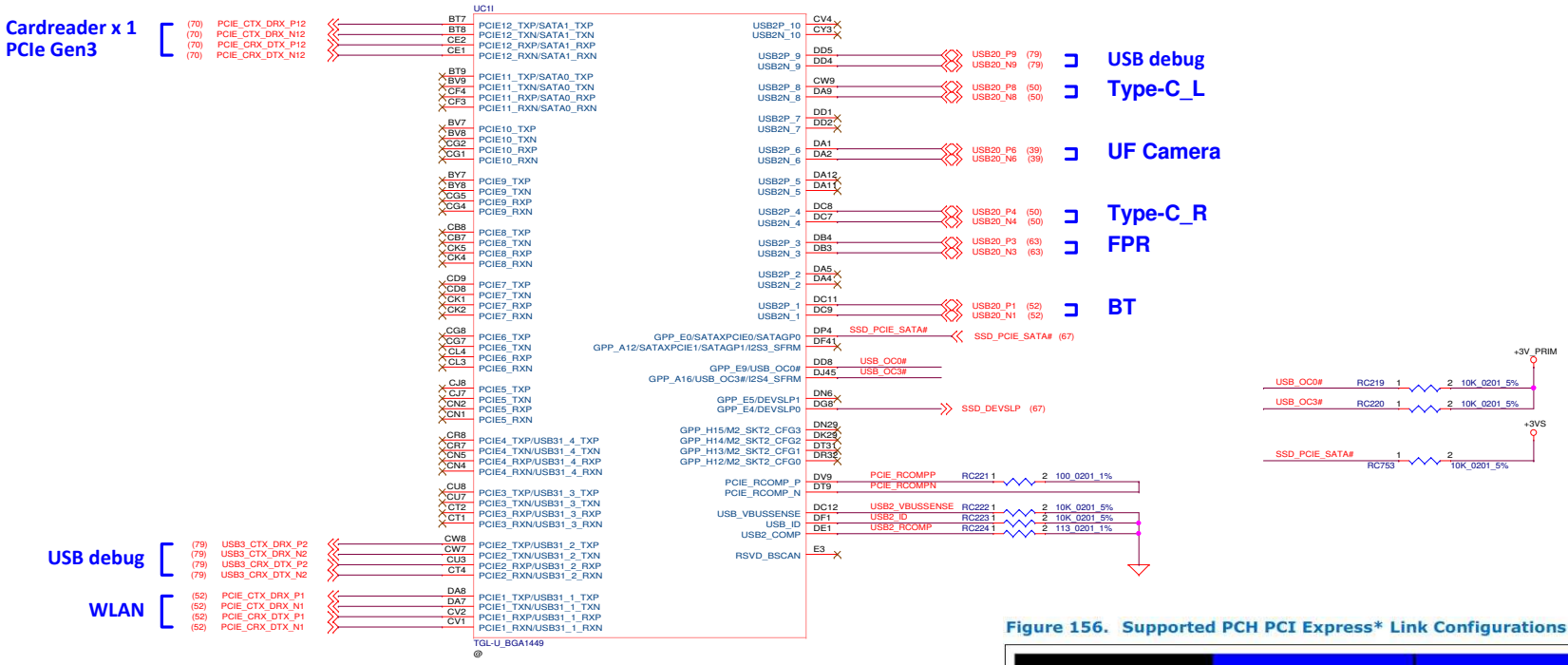
Compal Electronics, Inc.	
Title	P011 - TGL-U(6/13)CLK,GPIO
Size	Document Number: LA-J141P
Rev	0.1 (X00)
Date:	Tuesday, July 14, 2020
Sheet	11 of 100



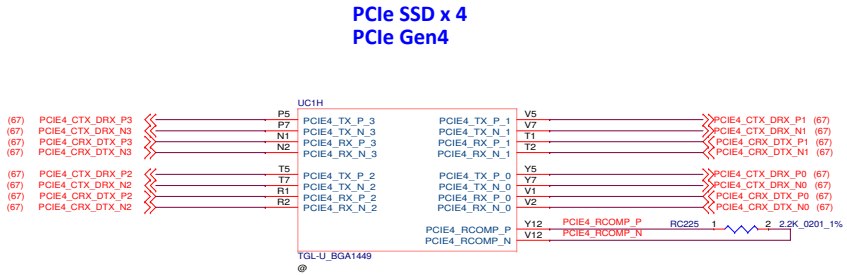


Figure 156. Supported PCH PCI Express* Link Configurations

PCH-LP		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3			
Flex I/O Lanes		0	1	2	3	4	5	6	7	8	9	10	11
PCIe* Lanes		1	2	3	4	5	6	7	8	9	10	11	12
Link Lanes	1x4	0	1	2	3	0	1	2	3	0	1	2	3
	1x4 LR	3	2	1	0	3	2	1	0	3	2	1	0
	2x2	0	1	0	1	0	1	0	1	0	1	0	1
	1x2+2x1	0	1	0	0	0	1	0	0	0	1	0	0
	2x1+1x2	0	0	1	0	0	0	1	0	0	0	1	0
	4x1	0	0	0	0	0	0	0	0	0	0	0	0
Base-U	1x4					RP5				RP9			
	1x4 LR					RP5				RP9			
	2x2					RP5		RP7		RP9		RP11	
	1x2+2x1					RP5		RP7	RP8	RP9		RP11	RP12
	2x1+1x2					RP8	RP7	RP5		RP12	RP11	RP9	
	4x1					RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12
Premium-U	1x4	RP1				RP5				RP9			
	1x4 LR	RP1				RP5				RP9			
	2x2	RP1		RP3		RP5		RP7		RP9		RP11	
	1x2+2x1	RP1		RP3	RP4	RP5		RP7	RP8	RP9		RP11	RP12
	2x1+1x2	RP4	RP3	RP1		RP8	RP7	RP5		RP12	RP11	RP9	
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12
Premium-Y	1x4	RP1								RP9			
	1x4 LR	RP1								RP9			
	2x2	RP1		RP3				RP7		RP9		RP11	
	1x2+2x1	RP1		RP3	RP4			RP7	RP8	RP9		RP11	RP12
	2x1+1x2	RP4	RP3	RP1						RP12	RP11	RP9	
	4x1	RP1	RP2	RP3	RP4			RP7	RP8	RP9	RP10	RP11	RP12

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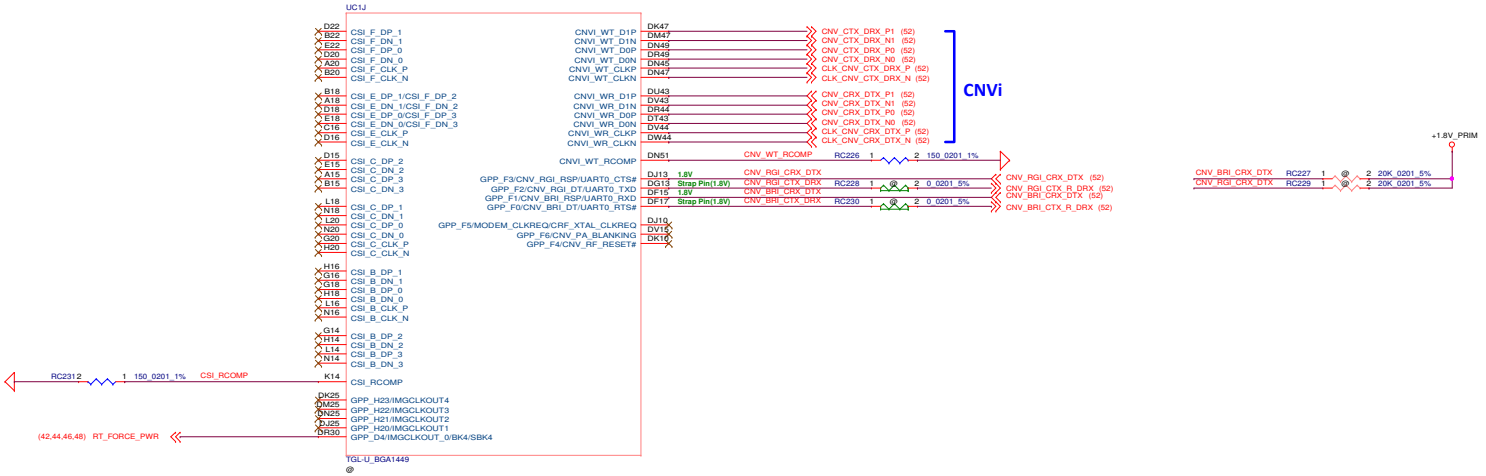
Compal Electronics, Inc.

Title: P012 - TGL-U(7/13)PCIE,USB

Size: | Document Number: LA-J141P | Rev: 0.1 (X00)

Date: Tuesday, July 14, 2020 | Sheet 12 of 100



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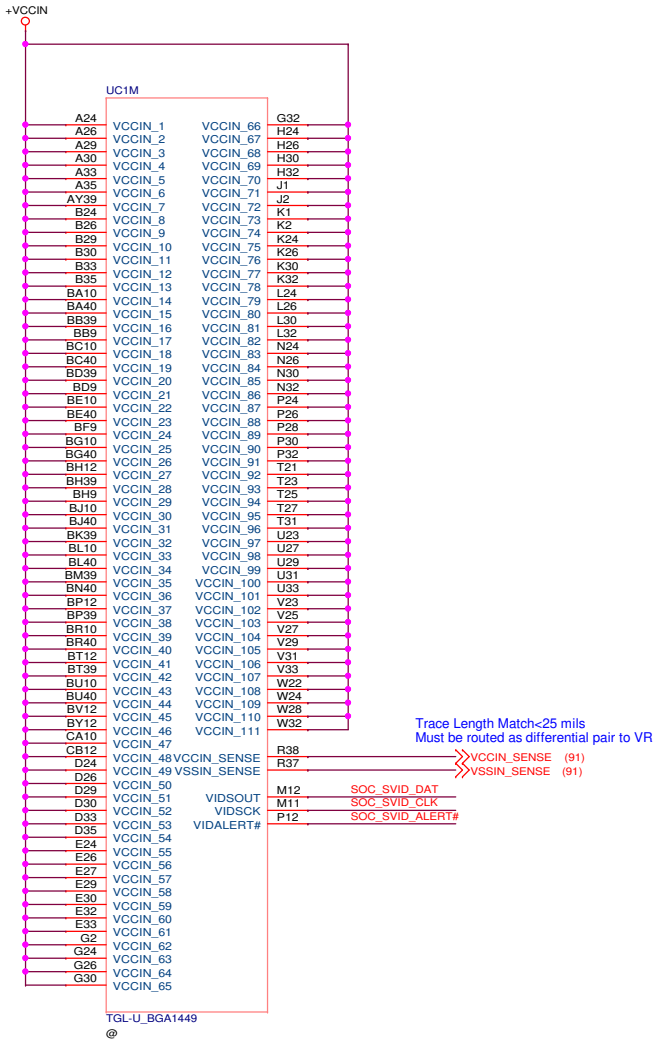
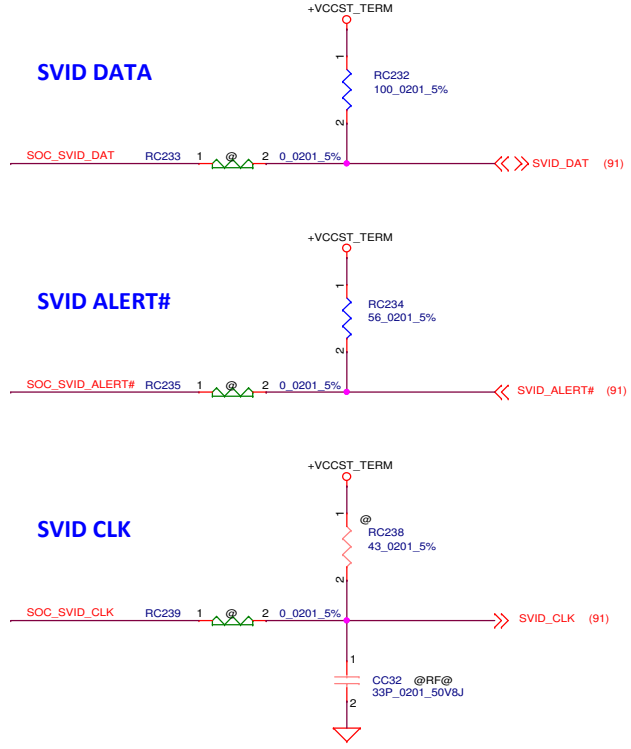
Compal Electronics, Inc.			
Title: P013 - TGL-U(8/13)CSI,CNVi			
Size	Document Number: LA-J141P		Rev: 0.1 (X00)
Date: Tuesday, July 14, 2020		Sheet 13 of 100	



1.The total Length of Data and Clock (from CPU to each VR) must be equal (¡Ó0.1 inch).
2.Route the Alert signal between the Clock and the Data signals.
CAD Note: Place the PU resistors close to CPU



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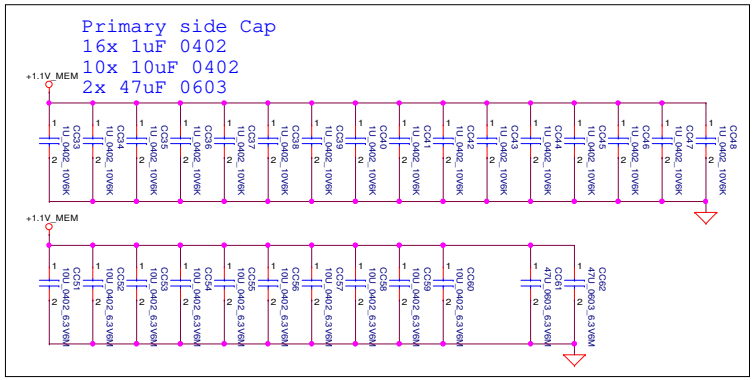
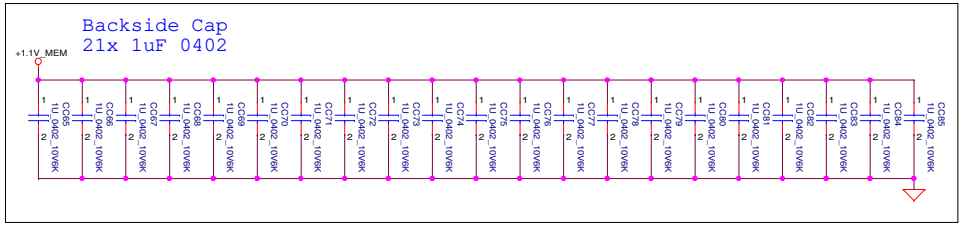
Compal Electronics, Inc.

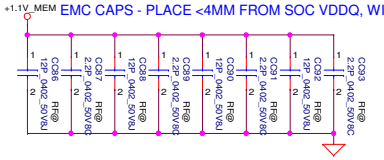
Title: P014 - TGL-U(9/13)CPU PWR,SVID

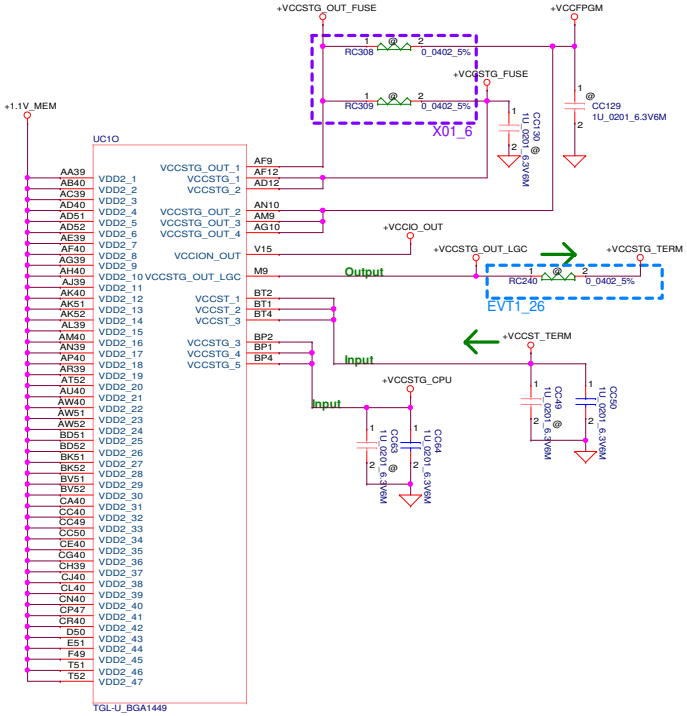
Size	Document Number	Rev
	LA-J141P	0.1 (X00)

Date: Tuesday, July 14, 2020 Sheet 14 of 100









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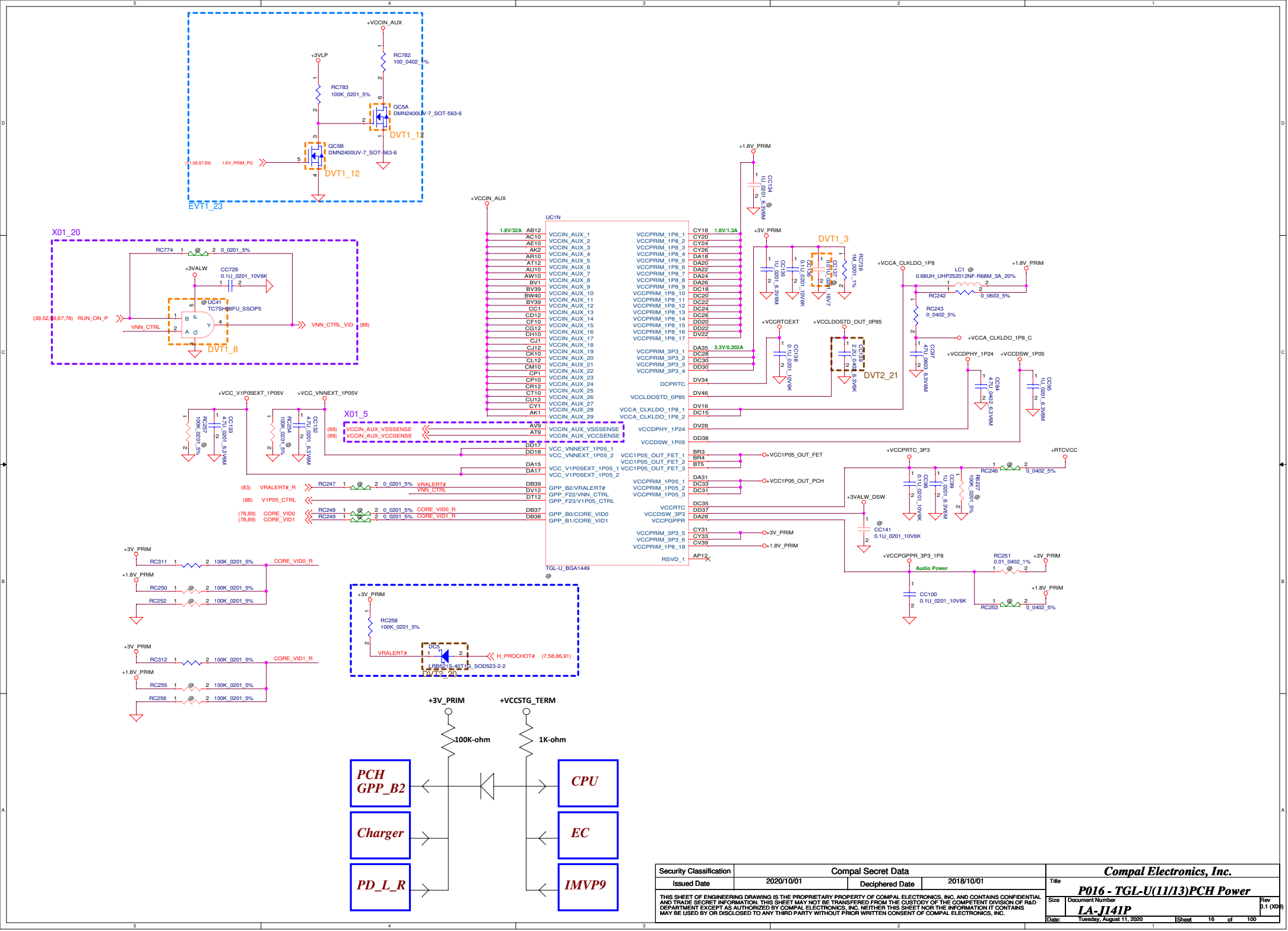
Compal Electronics, Inc.	
Title	P015 - TGL-U(10/13)CPU PWR
Size	Document Number: LA-J141P
Rev	0.1 (X00)
Date: Tuesday, July 14, 2020	Sheet 15 of 100



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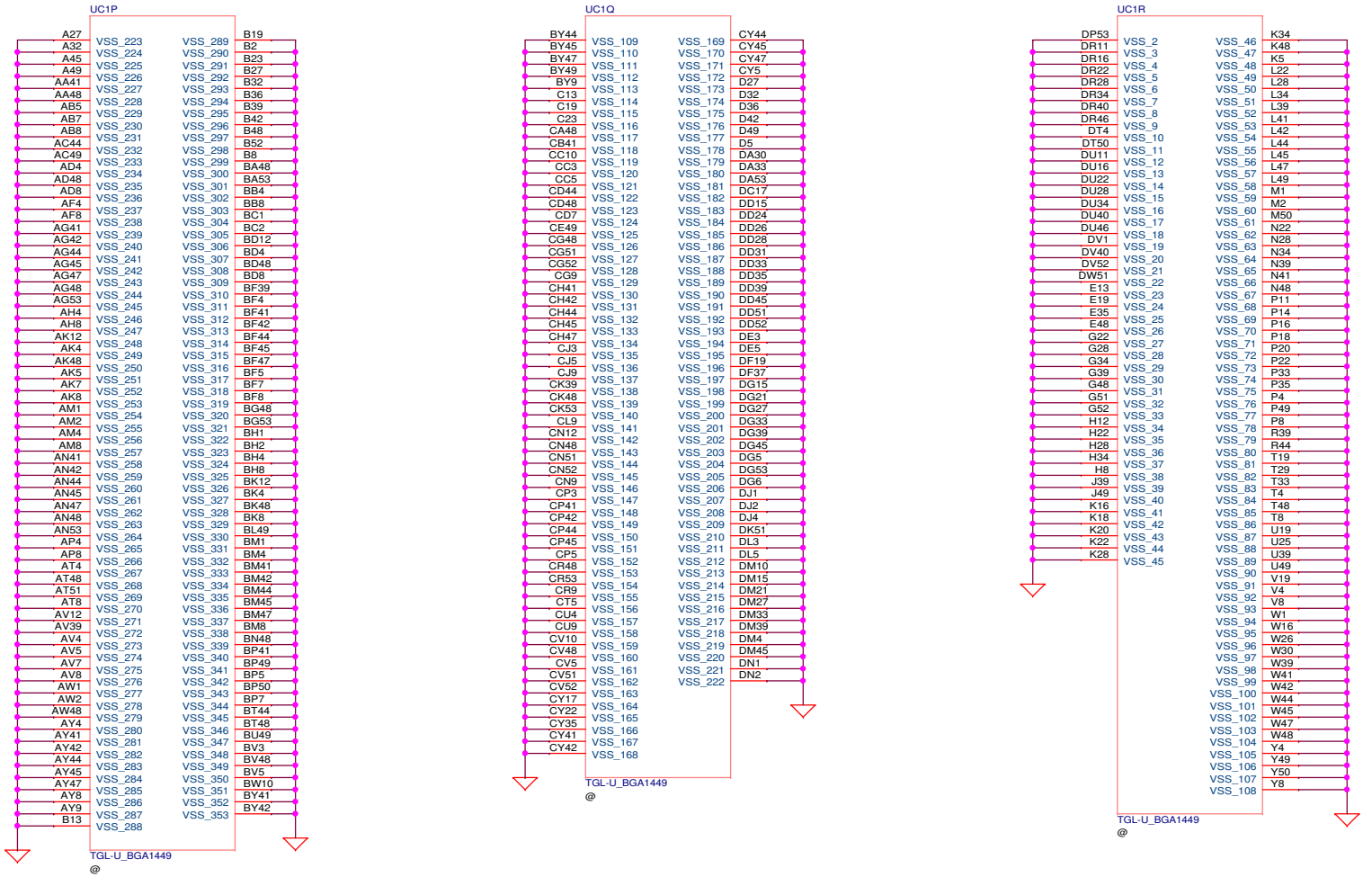
Compal Electronics, Inc.

Title: **P016 - TGL-U(11/13)PCH Power**

Size	Document Number	Rev
	LA-J141P	0.1 (X00)

Date: Tuesday, August 11, 2020 | Sheet 16 of 100



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Compal Electronics, Inc.

Title: **P017 - TGL-U(12/13)GND**

Size	Document Number	Rev
	LA-J141P	0.1 (X00)

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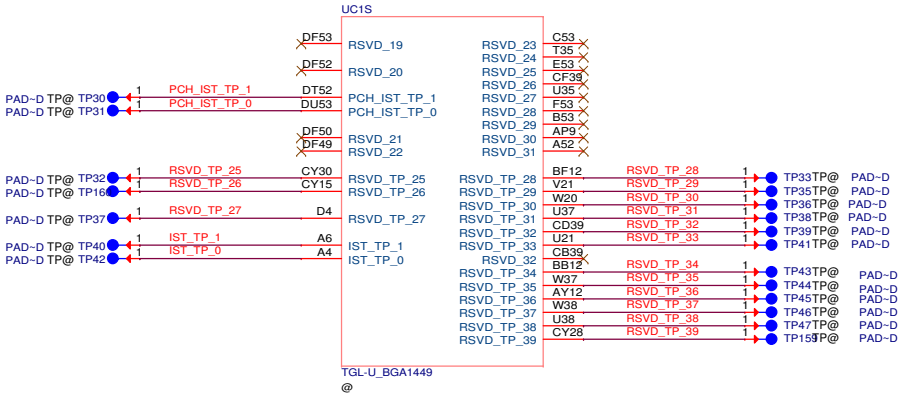

X01_19

DVT1_15

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Compal Electronics, Inc.

Title: **P018 - TGL-U(13/13)RSVD**

Size	Document Number	Rev
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Title: **P019 - Reserve**

Size	Document Number	Rev
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Compal Electronics, Inc.

Title: **P020 - Reserve**

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Compal Electronics, Inc.

Title: **P021 - Reserve**

Size	Document Number	Rev
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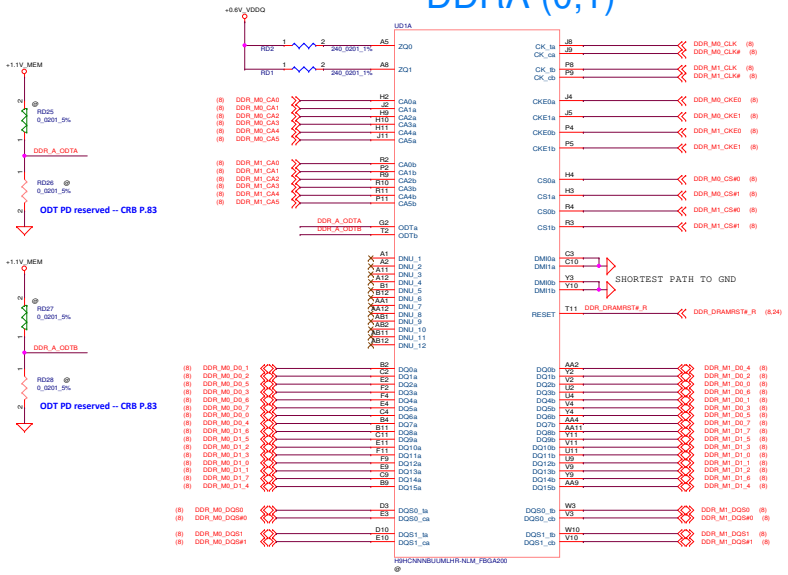
Title: **P022 - Reserve**

Size	Document Number	Rev
	LA-J141P	0.1 (X00)

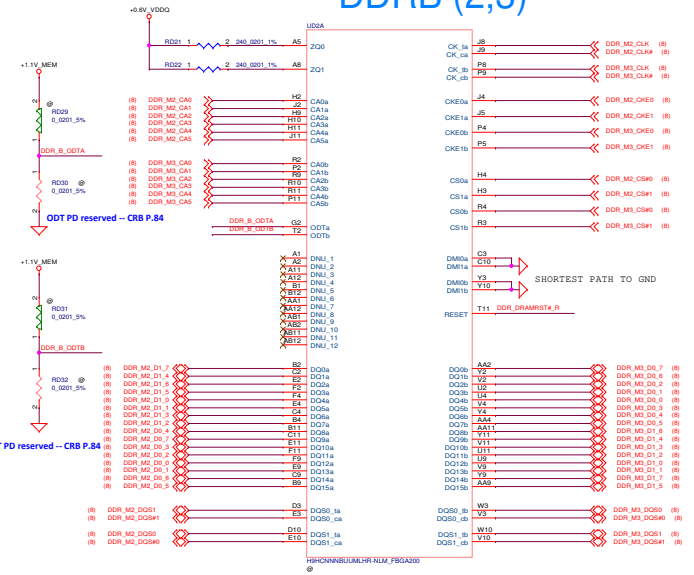
Date: Tuesday, July 14, 2020 | Sheet 22 of 100

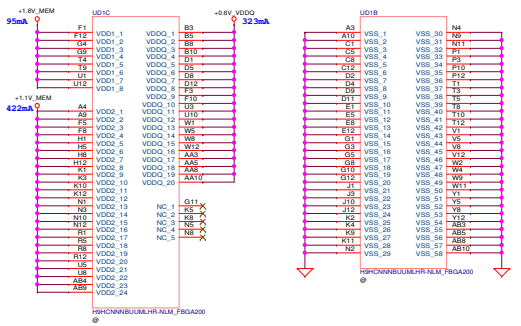
Memory connection refer 609182 REV0P5

DDRA (0,1)

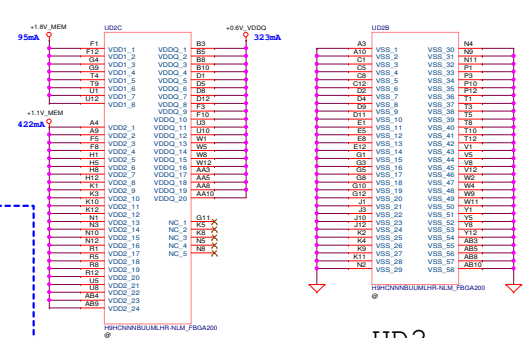


DDRB (2,3)

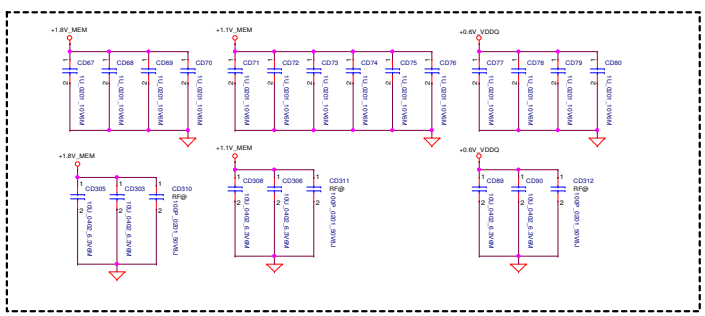


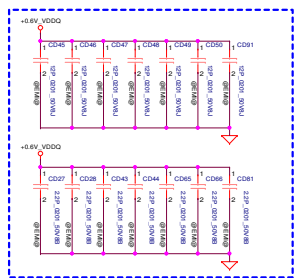


UD1

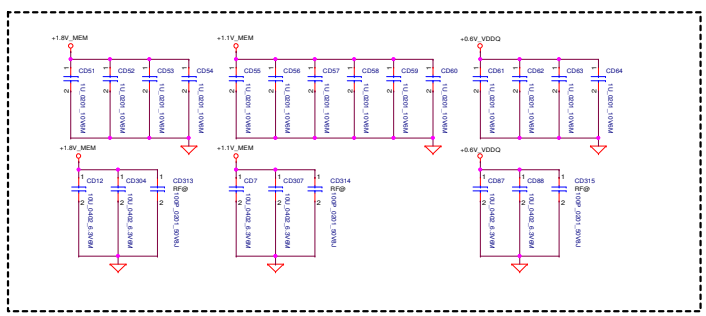


UD2





EMC CAPS



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			Size: Document Number: LA-J141P Rev: 3.1 (XX)
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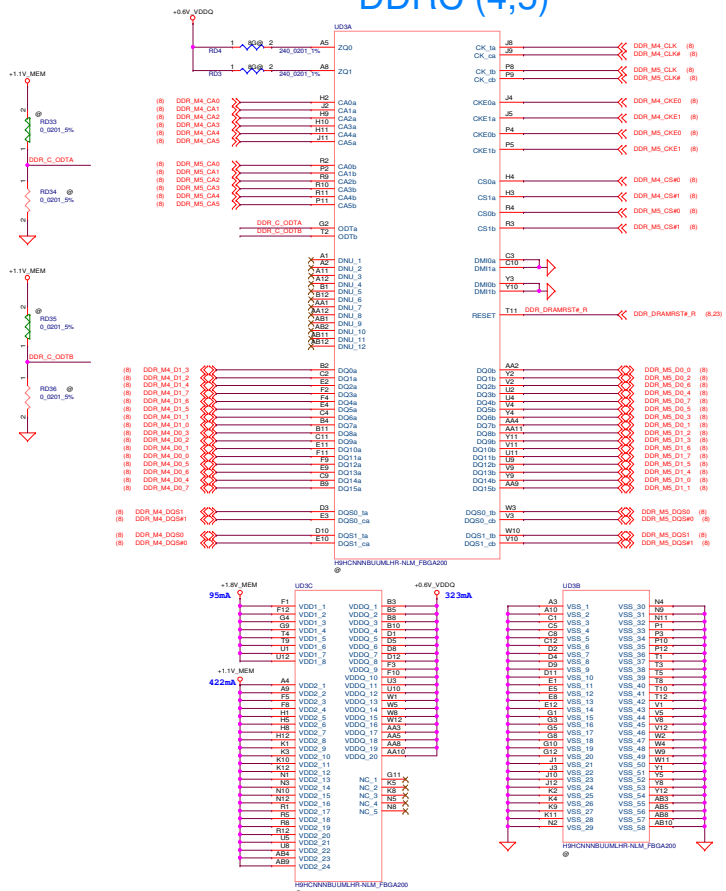
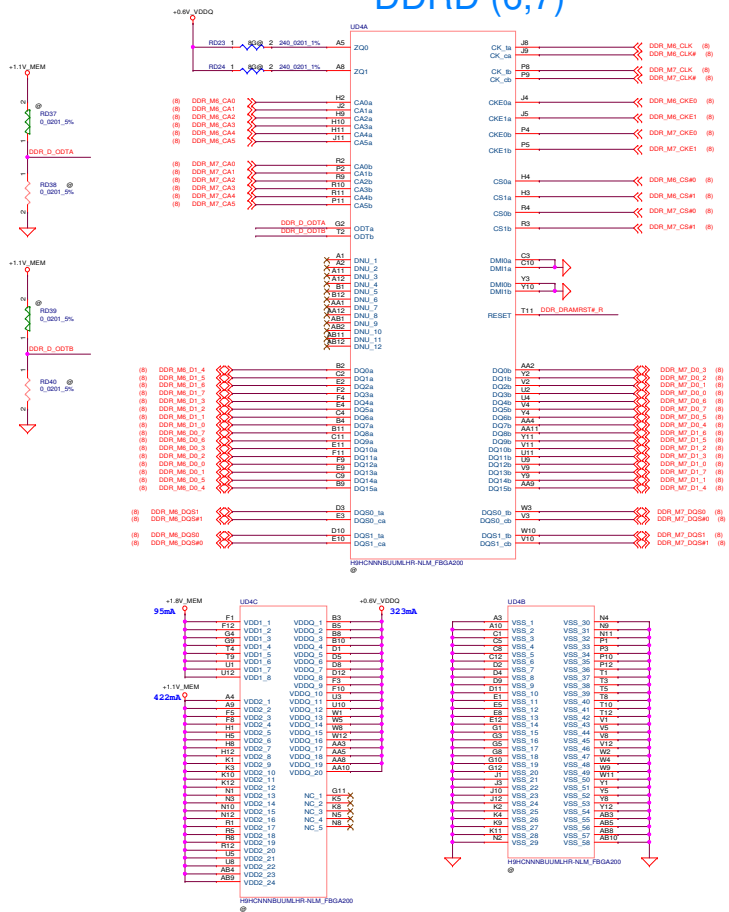
Memory connection refer 609182 REV0P5

DDRC (4,5)



DDRD (6,7)



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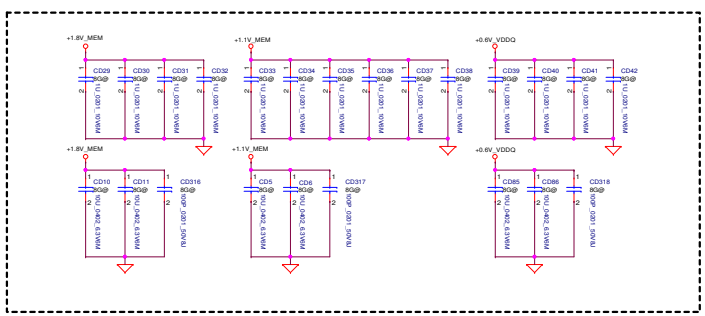

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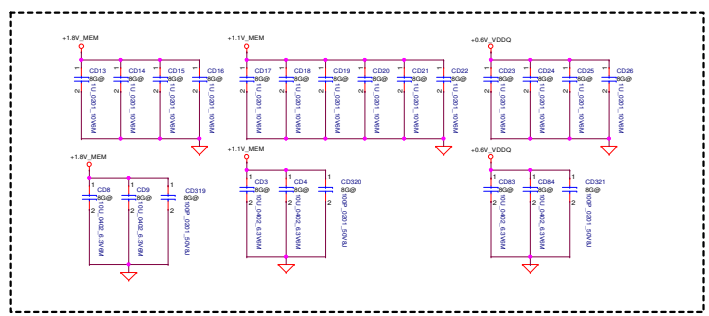

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			Size: Document Number: LA-J141P Rev: 3.1 (XX)
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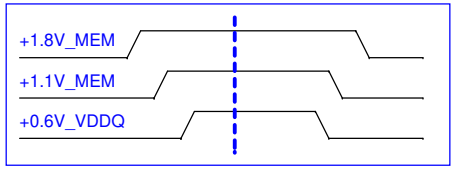
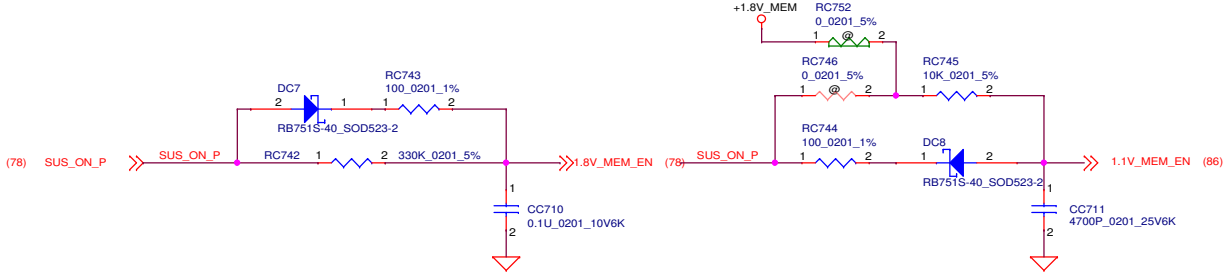
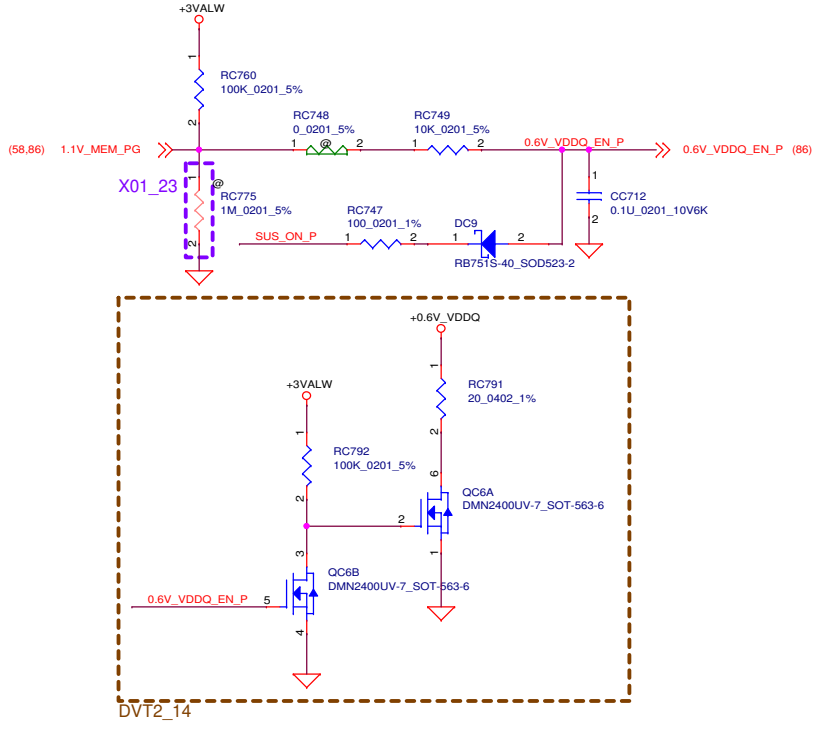
Follow Intel RVP for LP4x sequence







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Title: P025 - LPDDR4&4X BOM OPTION			
Size	Document Number: LA-J141P		Rev: 0.1 (X00)
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Title: **P034 - Reserve**

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Title: **P035 - Reserve**

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Title: **P036 - Reserve**

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Title: **P037 - Reserve**

Size	Document Number	Rev
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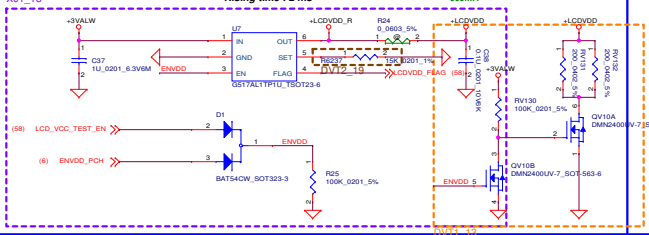
LCDVDD POWER

OCP: 1.6~1.8 A
RON : 70m ohm
VIH : 1.2V
Rising time : 2 ms

OCP
Continue current(A):Component Deratings:75%/Temperature Derating=80%
0.9A/0.75/0.8=1.5A

900mA

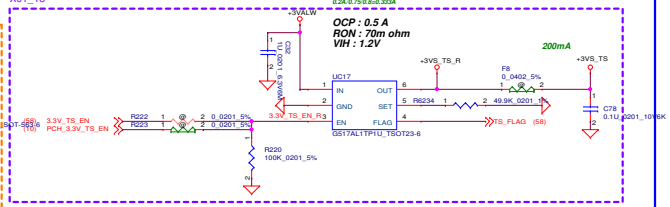


Touch Screen Power

OCP
Continue current(A):Component Deratings:75%/Temperature Derating=80%
0.2A/0.75/0.8=0.333A

OCP : 0.5 A
RON : 70m ohm
VIH : 1.2V

200mA

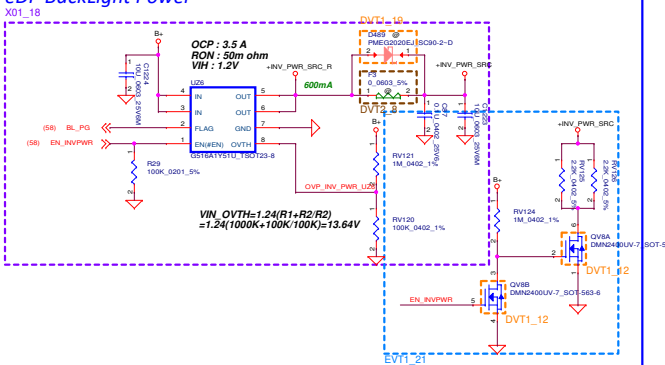


eDP BackLight Power

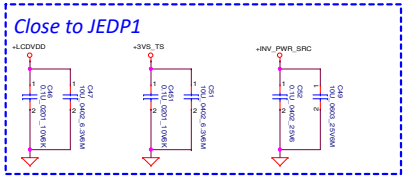
OCP : 3.5 A
RON : 50m ohm
VIH : 1.2V

600mA

VIN_OVTH=1.24(R1+R2/R2)
=1.24(1000K+100K/100K)=13.64V

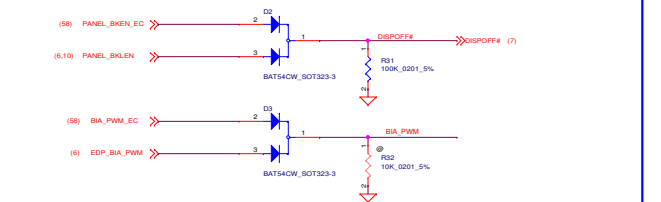


Close to JEDP1

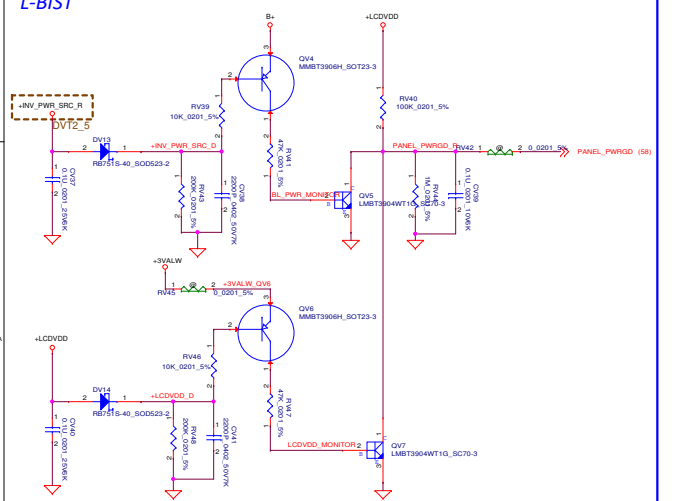


Close to JEDP1

BackLight PWM Control



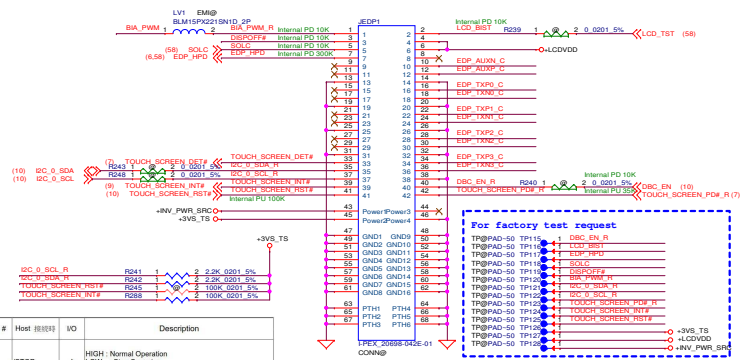
BL_PWR_SRC & LCDVDD monitor
L-BIST



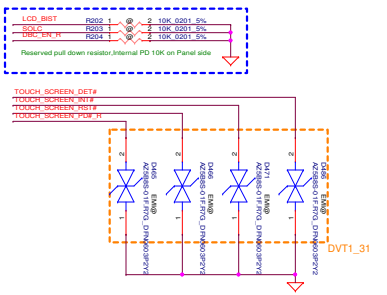
eDP* Bit Rates 8.1 Gb/s (HBR3)
In TCON side , RX Equalization is CTLE + DFE
DFE=Decision feedback equalizer
CTLE=Continuous Time Linear Equalizer

Table 5-41. eDP* Bit Rates

Bit Rate	Lane Supports (max # of lanes)	Peak Bandwidth
1.62 Gb/s (RBR)	4	4 x 162 MB/s = 648 MB/s
2.7 Gb/s (HBR)	4	4 x 270 MB/s = 1080 MB/s
5.4 Gb/s (HBR2)	4	4 x 540 MB/s = 2160 MB/s
8.1 Gb/s (HBR3)	4	4 x 810 MB/s = 3240 MB/s



CN1 PIN #	Host 接脚特	I/O	Description
1	/STOP	I	HIGH : Normal Operation LOW : Stop Scanning Build-in pullup (to 3.3 volts) resistor 35kohm
2	IIC SDA	I/O	IIC Data Open drain output; pull-up resister at Host is needed
3	IIC SCL	I	IIC Clock Open drain output; pull-up resister at Host is needed
4	NC	-	No Connection
5	NC	-	No Connection
6	/IIC IRQ	O	IIC Data Ready Output "LOW" when data ready to send Open drain output; pull-up resister at Host is needed
7	/RESET	I	Hardware RESET : Low Active Stop operation when pull "LOW" Build-in pull-up (to 3.3 volts) resister 100kohm
8	VDD +3.3V	-	3.3 volts (typ) power input
9	DGND	-	Ground
10	DGND	-	Ground



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Issued Date	2020/10/01	Deciphered Date 2018/10/01	Title: P038 - eDP,Touch Screen
			Size: Document Number: LA-J141P Rev: 0.1 (X00)
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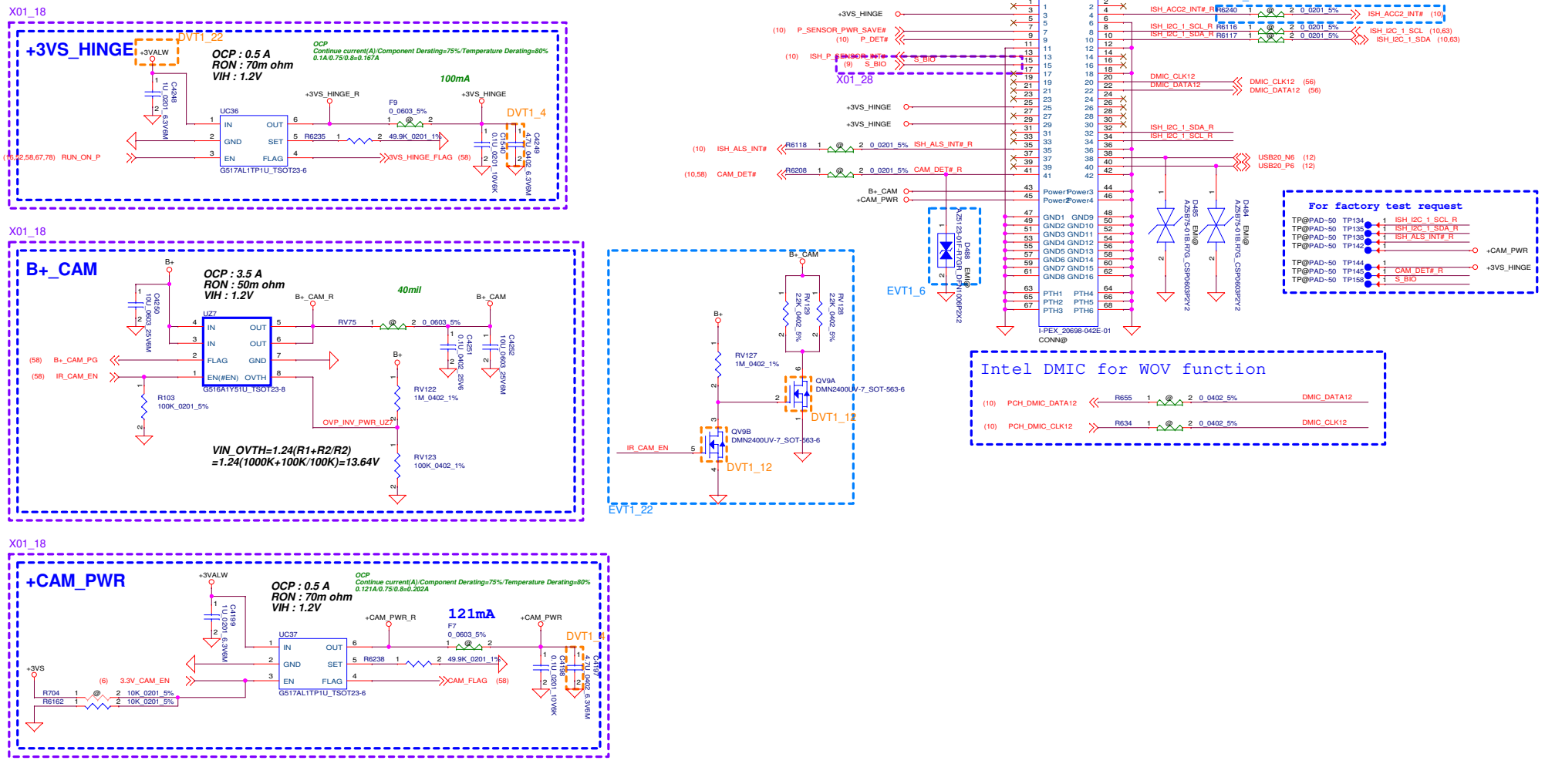

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Title: **P039 - UF Camera,MIC,ALS**

Size: | Document Number: **LA-J141P** | Rev: 0.1 (X00)

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Title: **P040 - Reserve**

Size	Document Number	Rev
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Title: **P041 - Reserve**

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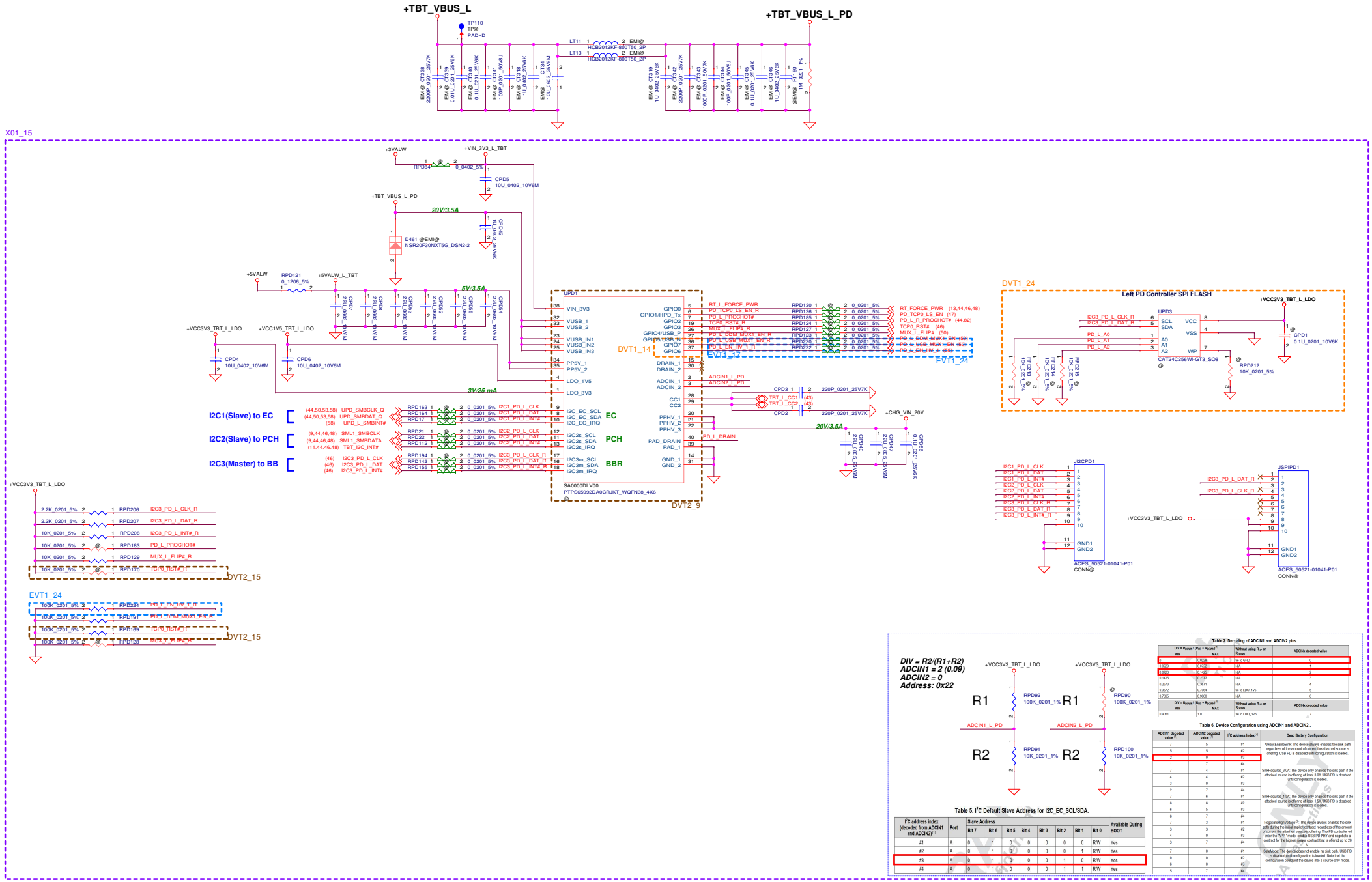

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Title	P042 - TYPE-C Port L_PD
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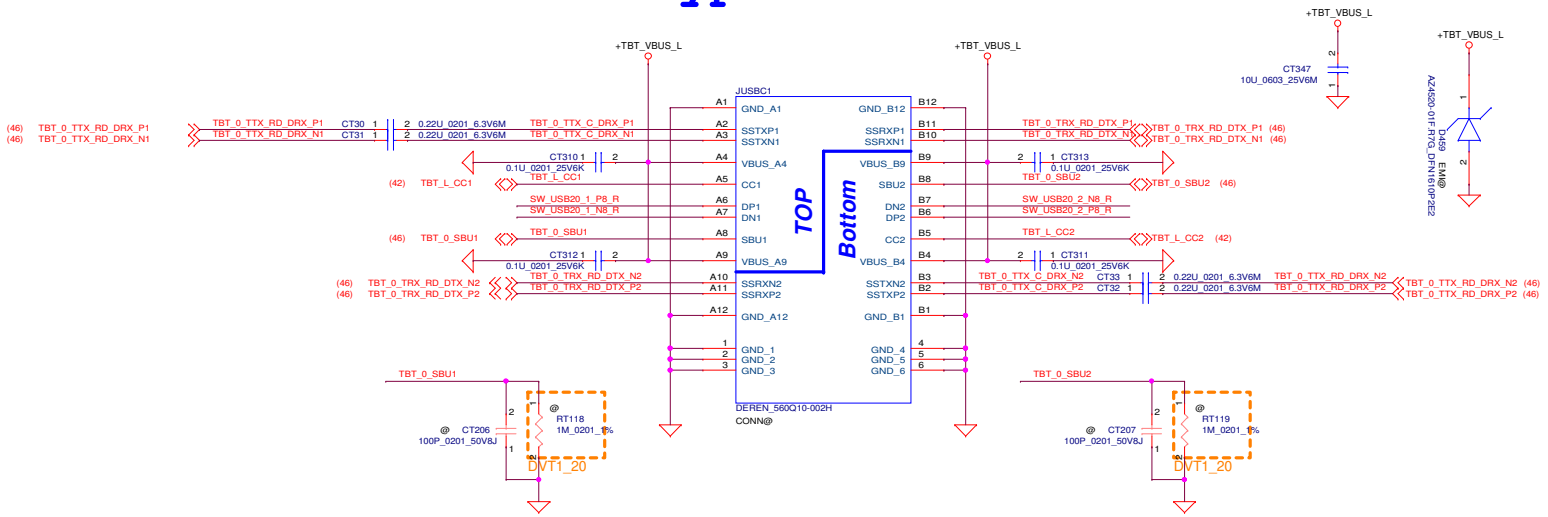
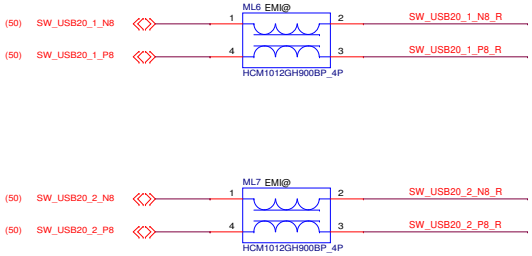
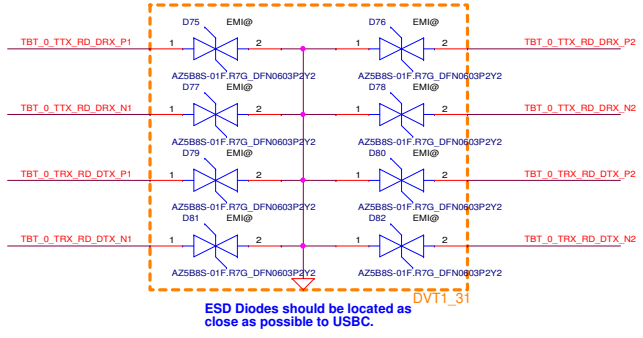
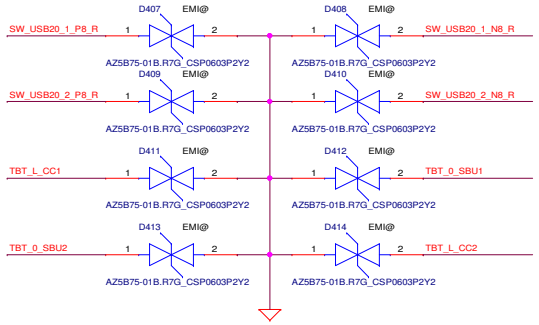
LEFT Type-C Connector

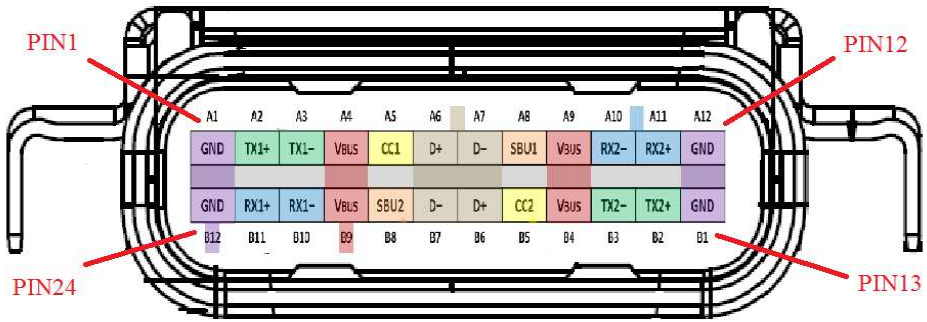






ESD Diodes should be located as close as possible to USBC.





Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

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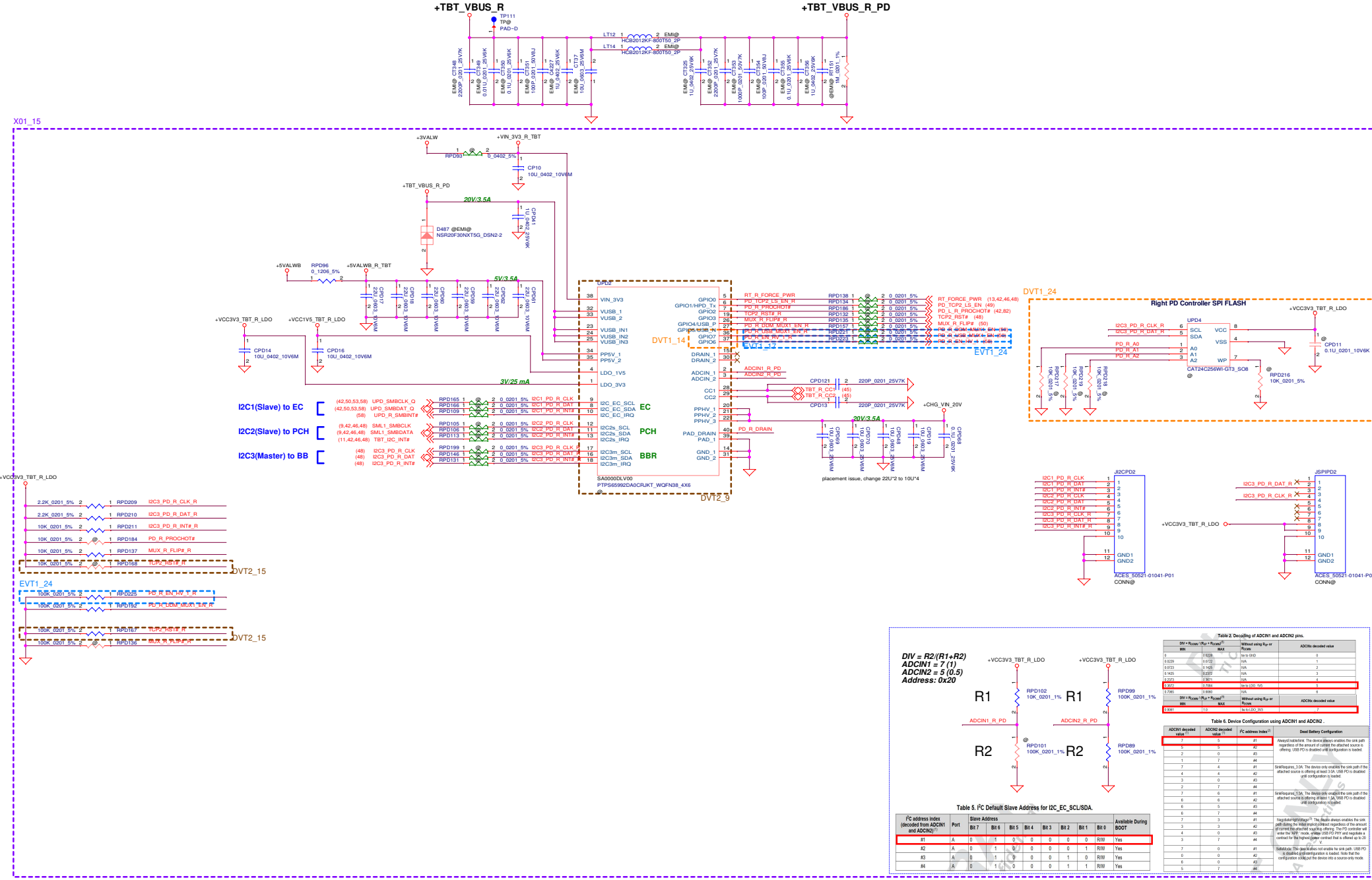
Compal Electronics, Inc.	
Title	P043 - TYPE-C Conn L
Size	Document Number: LA-J141P
Rev	0.1 (X00)
Date:	Tuesday, July 14, 2020
Sheet	43 of 100

Vendor confirmed completion on 3/20



Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

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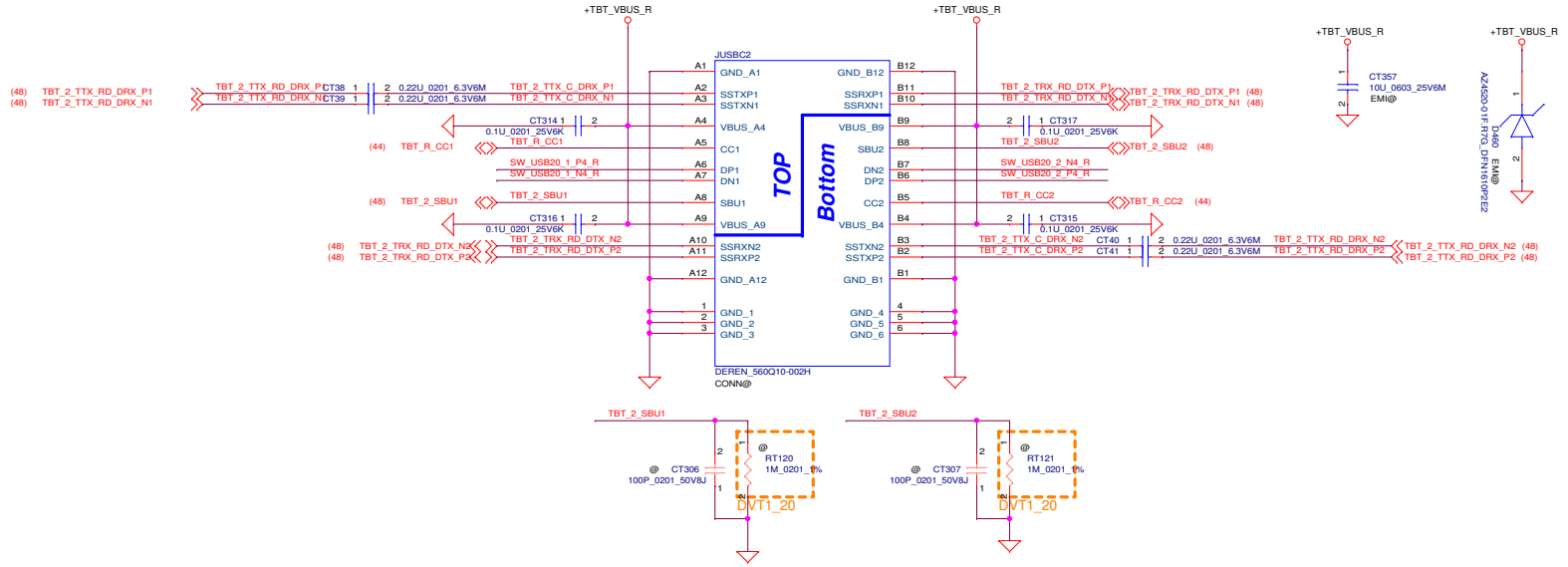
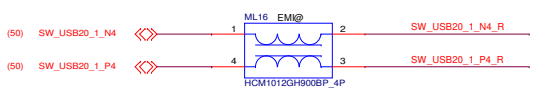
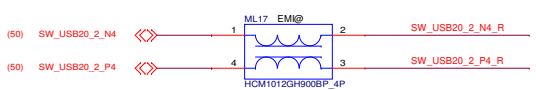
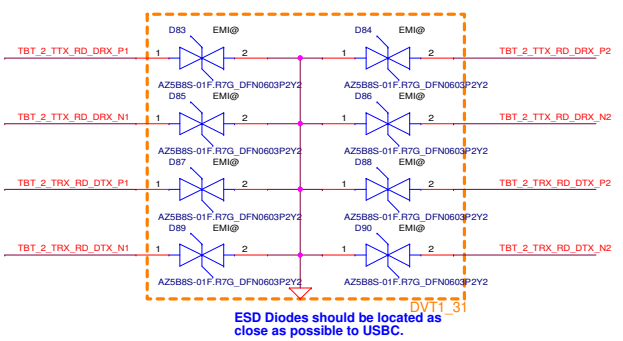
Compal Electronics, Inc.			
Title: P044 - TYPE-C Port R_PD			
Size	Document Number: LA-J141P		Rev: 0.1 (X00)
Date: Tuesday, July 14, 2020	Sheet 44 of 100		

RIGHT Type-C Connector

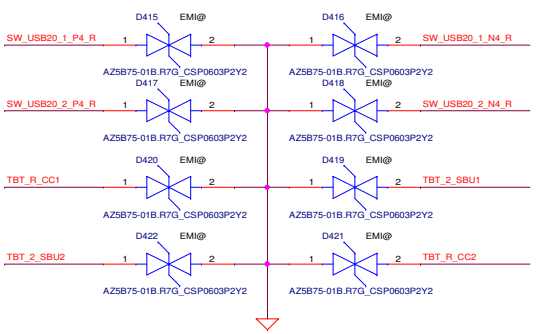


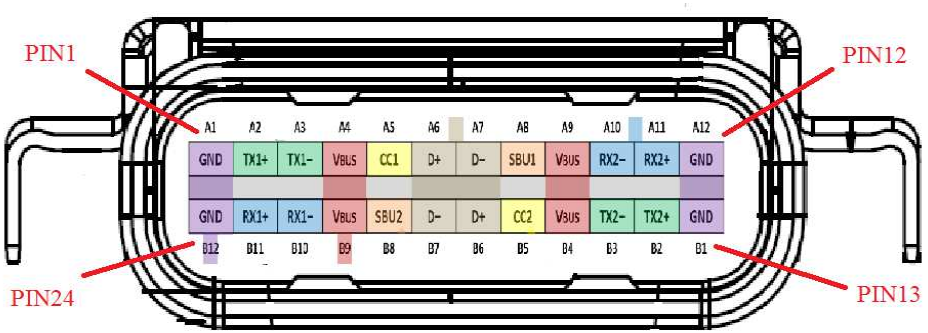






ESD Diodes should be located as close as possible to USBC.





Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

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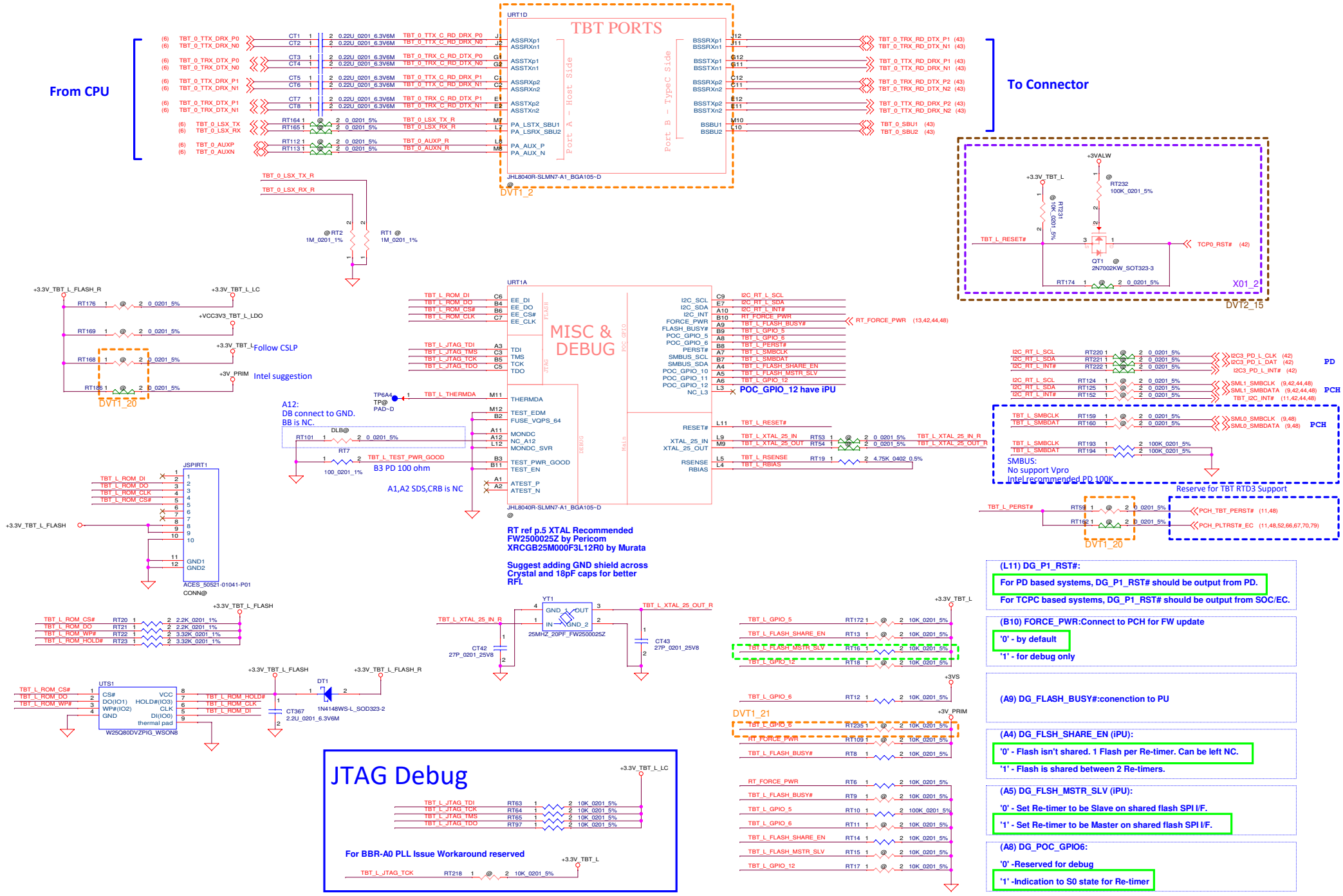
Compal Electronics, Inc.	
Title	P045 - TYPE-C Conn R
Size	Document Number: LA-J141P
Rev	0.1 (X00)
Date: Tuesday, July 14, 2020	Sheet 45 of 100



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Issued Date	2020/10/01	Deciphered Date 2018/10/01

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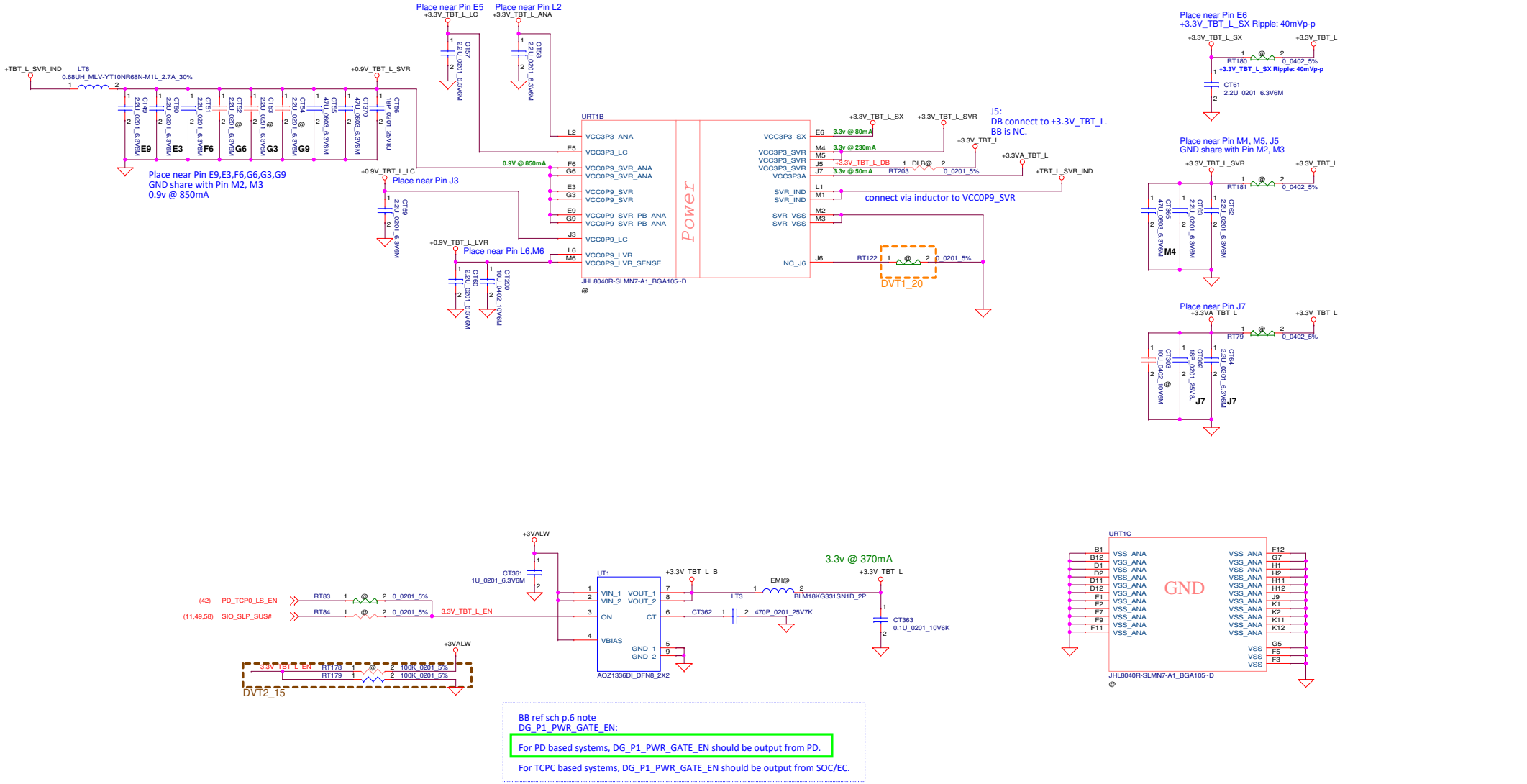
Compal Electronics, Inc.

Title: **P046 - TYPE-C TBT_BB L_TCSS**

Size: | Document Number: **LA-J141P** | Rev: 0.1 (X00)

Date: Tuesday, July 14, 2020 | Sheet 46 of 100



Security Classification	Compal Secret Data	
Issued Date	2020/10/01	Deciphered Date 2018/10/01

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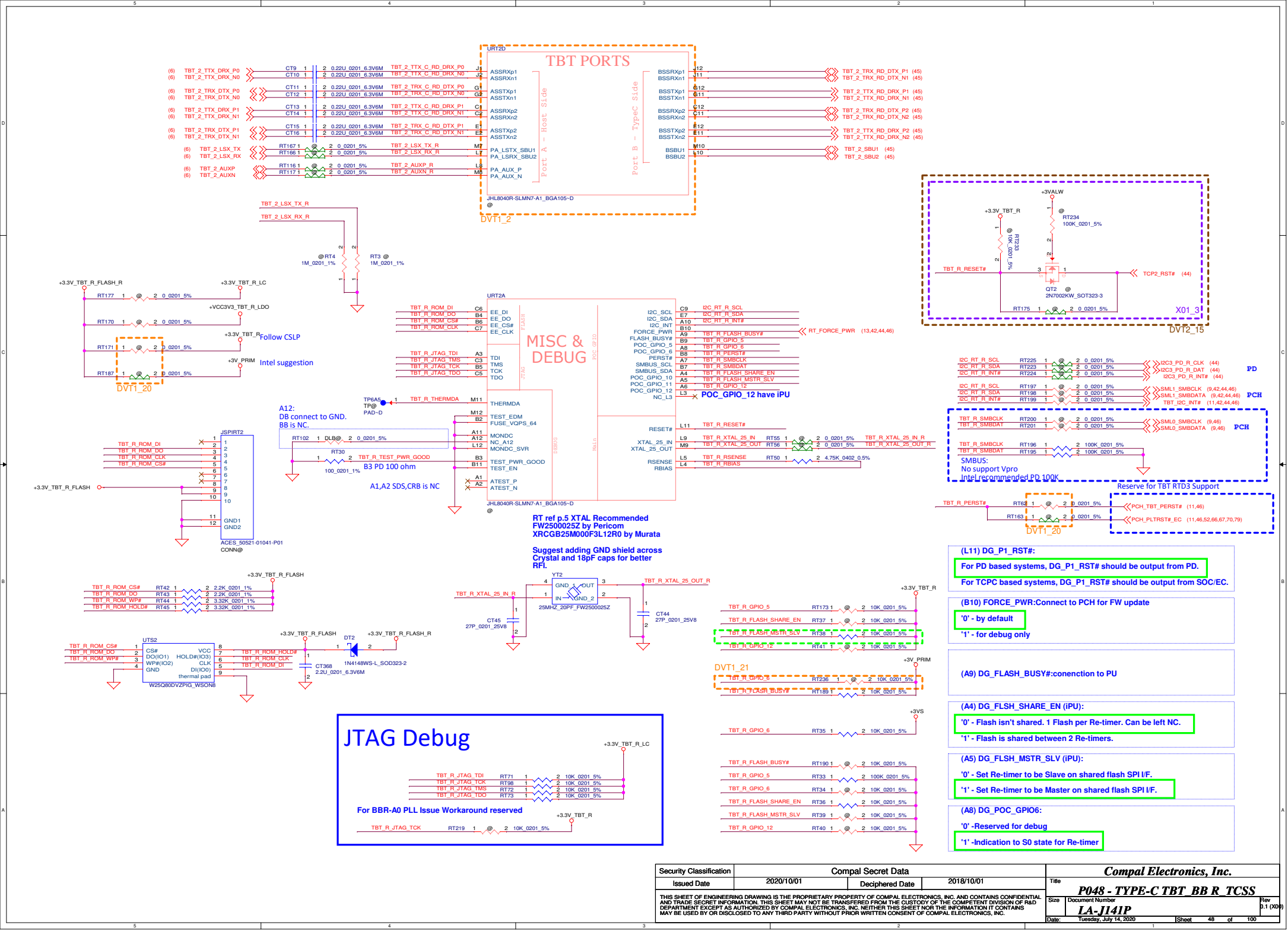
Compal Electronics, Inc.

Title: P047 - TYPE-C TBT_BB L_PWR,GND

Size: LA-J141P | Document Number | Rev 0.1 (X00)

Date: Tuesday, July 14, 2020 | Sheet 47 of 100



Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

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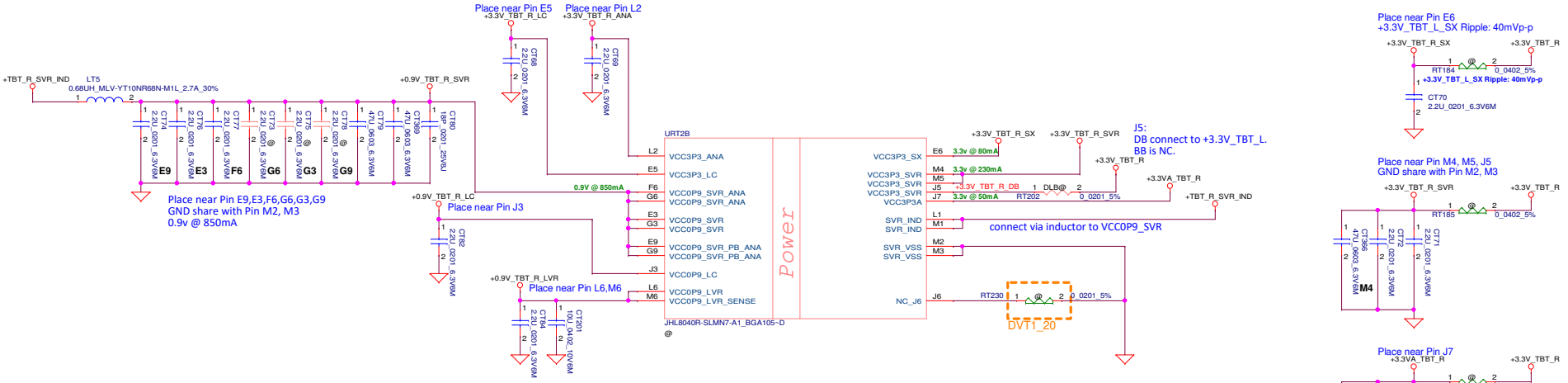
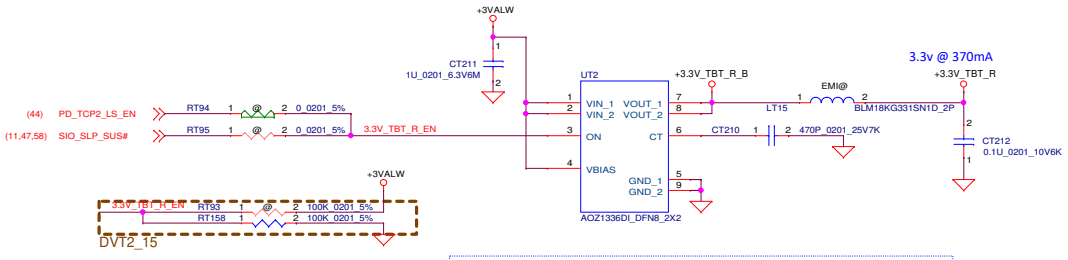
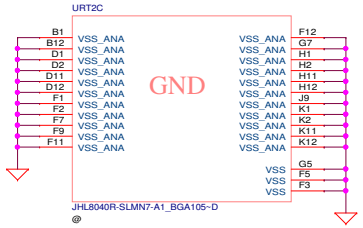
Compal Electronics, Inc.			
Title	P048 - TYPE-C TBT_BB R_TCSS		
Size	Document Number		Rev
	LA-J141P		0.1 (X00)
Date:	Tuesday, July 14, 2020	Sheet	48 of 100







Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

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Compal Electronics, Inc.

Title: **P049 - TYPE-C TBT_BB R_PWR,GND**

Size	Document Number	Rev
	LA-J141P	0.1 (X00)

Date: Tuesday, July 14, 2020 Sheet 49 of 100

USB2/I2C MUXES_L

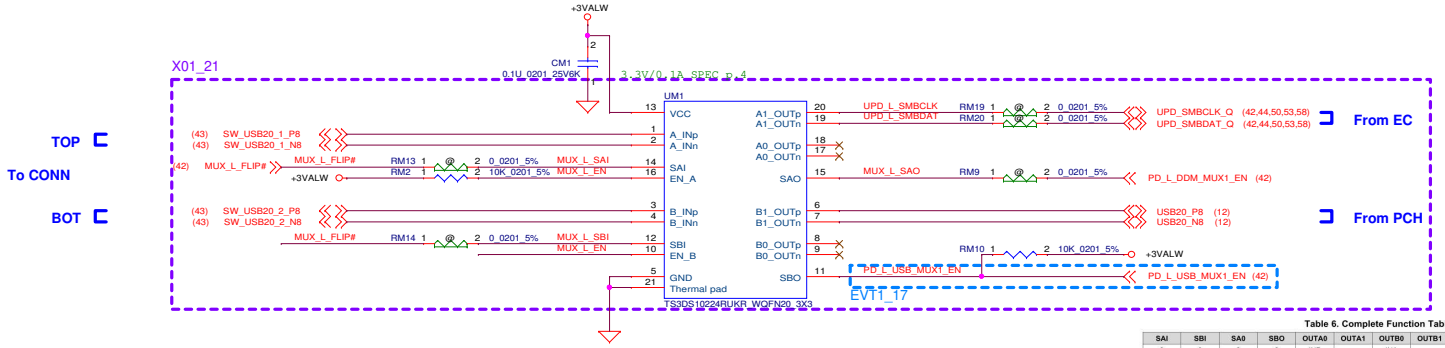
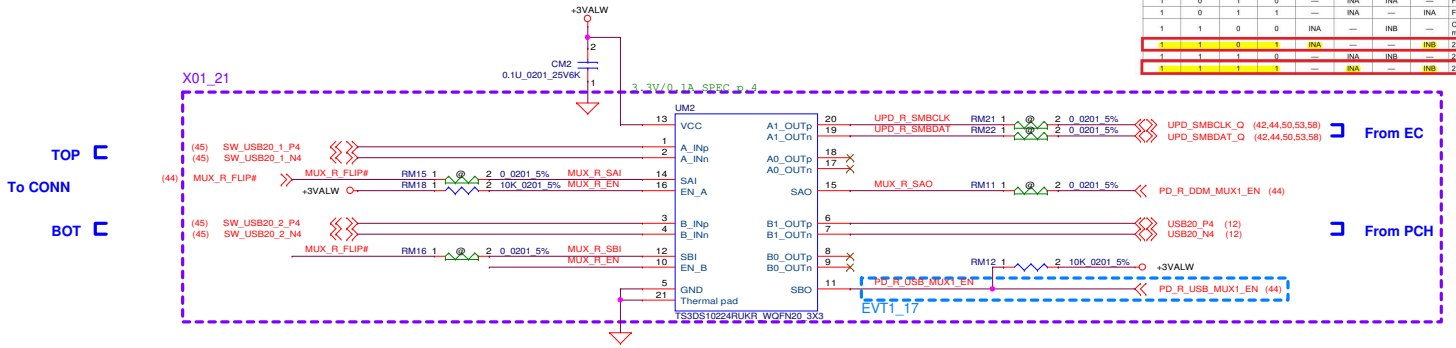


Table 6. Complete Function Table

SAI	SBI	SA0	SBO	OUTA0	OUTA1	OUTB0	OUTB1	FUNCTIONAL MODE	
0	0	0	0	INB	—	INA	—	Crosspoint, 1-channel 1:4 mux	
0	0	0	1	INB	—	—	INA	1-channel 1:4 mux	USB only on TBT_A_TOP_P/N
0	0	1	0	—	INB	INA	—	1-channel 1:4 mux	
0	0	1	1	—	INB	—	INA	1-channel 1:4 mux	USB on TBT_A_TOP_P/N; DDM on TBT_A_BOT_P/N
0	1	0	0	INB	—	INA	—		
0	1	0	1	INB	—	—	INA		
0	1	1	0	—	INB	INB	—		
0	1	1	1	—	INB	—	INB		
1	0	0	0	INA	—	INA	—	Fan-out 1:2 configuration	
1	0	0	1	INA	—	—	INA	Fan-out 1:2 configuration	
1	0	1	0	—	INA	INA	—	Fan-out 1:2 configuration	
1	0	1	1	—	INA	—	INA	Fan-out 1:2 configuration	
1	1	0	0	INA	—	INB	—	Crosspoint, 2-channel 1:2 mux, 1-channel 1:4 mux	
1	1	0	1	INA	—	—	INB	2-channel 1:2 mux,1-channel 1:4 mux	USB only on TBT_A_BOT_P/N
1	1	1	0	—	INA	INB	—	2-channel 1:2 mux,1-channel 1:4 mux	
1	1	1	1	—	INA	—	INB	2-channel 1:2 mux,1-channel 1:4 mux	USB on TBT_A_BOT_P/N; DDM on TBT_A_TOP_P/N

USB2/I2C MUXES_R



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Issued Date	2020/10/01	Deciphered Date	2018/10/01

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Compal Electronics, Inc.

Title: **P050 - TYPE-C USB/I2C MUX**

Size: | Document Number: **LA-J141P** | Rev: 0.1 (X00)

Date: Tuesday, July 14, 2020 | Sheet 50 of 100

Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

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Compal Electronics, Inc.

Title: **P051 - Reserve**

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WLAN Power
FAN_R Power

Max Current : 6A
RON : 20m ohm
VIH : 1.2V

C_{TX} (pF)	Rise Time (µs) 10%~90%, C_{LK}=0.1µF, C_{INK}=1µF, R_{TX}=10Ω Typical Values at 25°C, 25V X7R 10% Ceramic Cap.						
	V_{INK}=5V	3.3V	1.8V	1.5V	1.2V	1.05V	0.8V
0	85	68	49	45	40	37	34
220	431	297	172	147	122	106	89
470	888	583	332	269	218	189	161
1000	1700	1130	657	550	446	390	316
2200	3805	2534	1347	1152	966	867	701
4700	8053	5255	1997	2578	2101	1838	1483
10000	18330	12050	5545	5545	4155	4155	3329

Reserved for CNVi power control

M.2 CNVI MODES

GPP_F2/CNV_RGI_DT

0 = INTEGRATED CNVI ENABLE

1 = INTEGRATED CNVI DISABLE

XTAL SEL

GPP_F0/CNV_BRI_DT (Internal 20 K Pull Down)

0 = 38.4/19.2MHZ (DEFAULT)

1 = 24MHZ (25 MHZ WHEN XTAL FREQ DIVIDER NON ZERO)

NO support C-Link

REFCLK0 use by Jefferson Peak

pull up on EC side

CNVi=3.3V

PCIe=1.8V

open drain

Security Classification	Compal Secret Data
Issued Date	2020/10/01
Deciphered Date	2018/10/01

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Compal Electronics, Inc.

Title: P052 - WLAN/BT (w/ CNVi)

Size: — Document Number: LA-J141P — Rev: 0.1 (X00)

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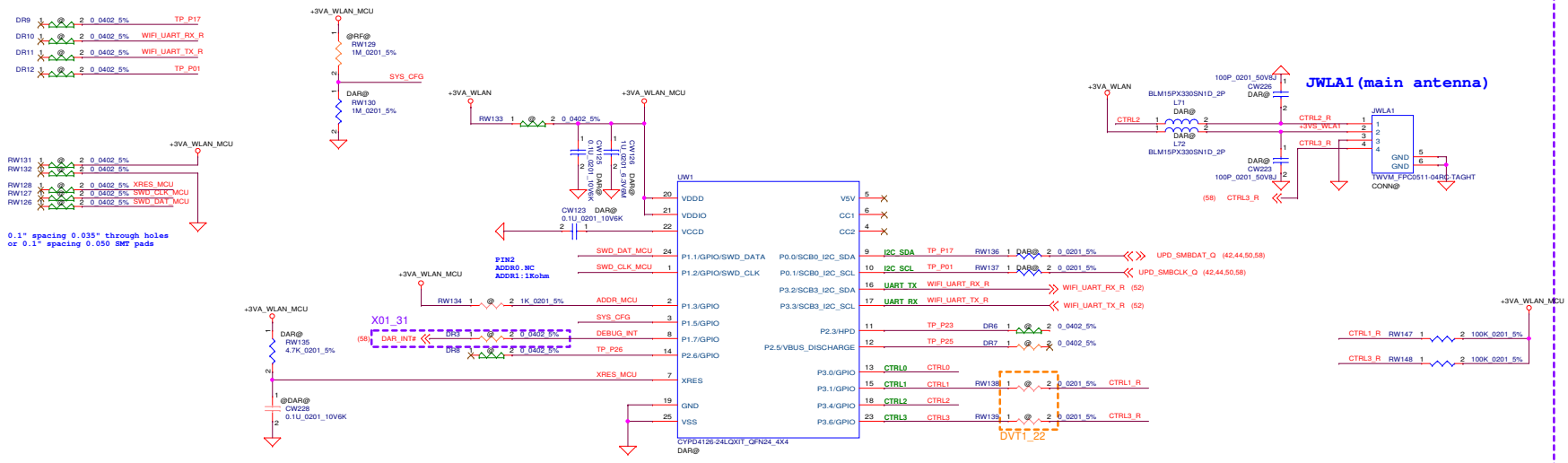
X01_13

Darwin 2.0



I2C ADDR	I2C Slave Address
NC	0x72 (default)
Pull up 3.3V	0x34

Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

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Compal Electronics, Inc.	
Title	P053 - Darwin
Size	Document Number: LA-J141P
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Date:	Tuesday, July 14, 2020
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Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **P054 - Reserve**

Size	Document Number	Rev
	LA-J141P	0.1 (X00)

Date: Tuesday, July 14, 2020 | Sheet 54 of 100

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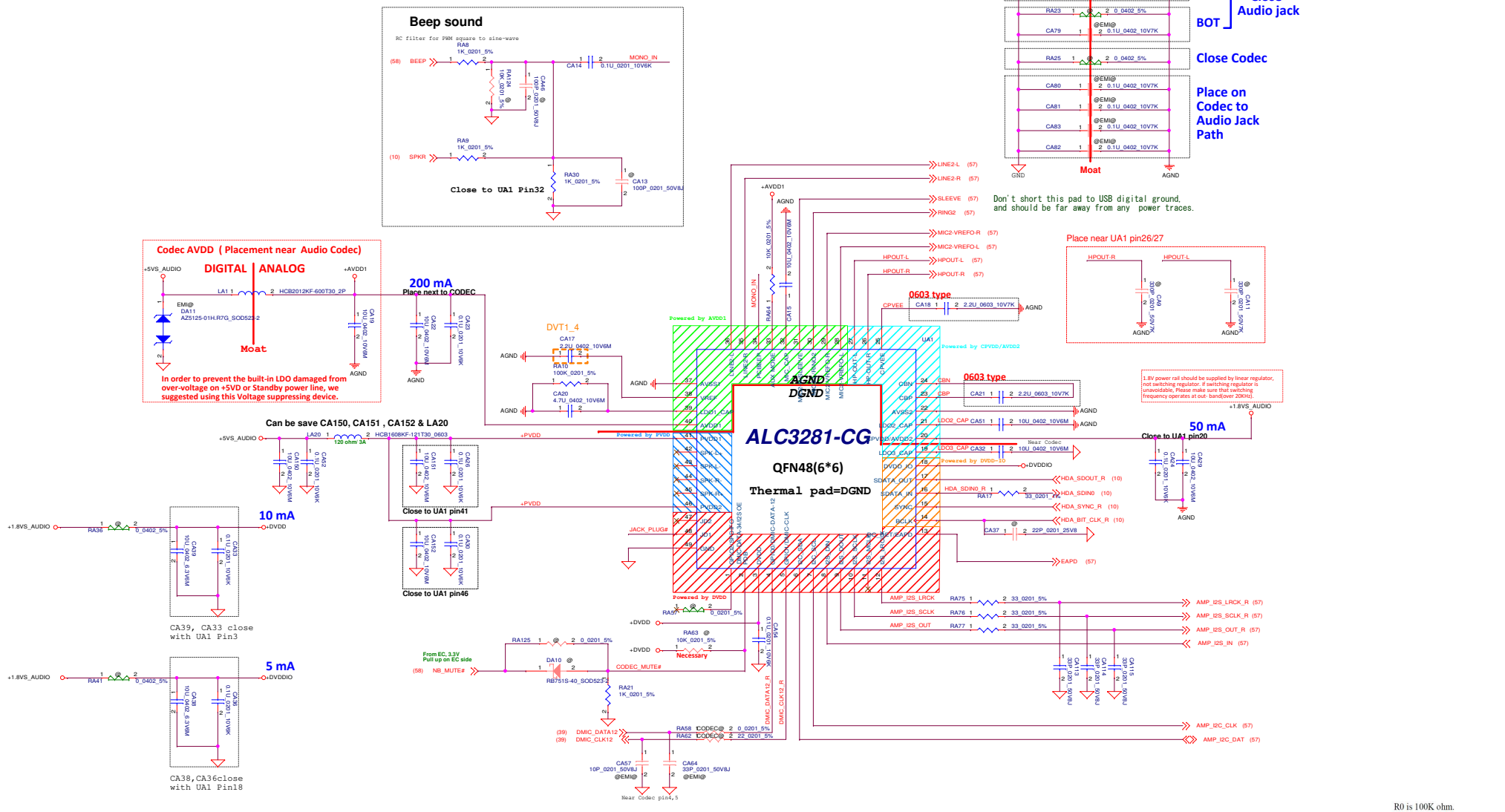
Compal Electronics, Inc.

Title: **P055 - Reserve**

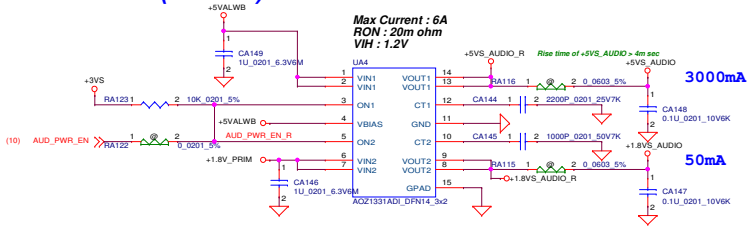
Size	Document Number	Rev
	LA-J141P	0.1 (X00)

Date: Tuesday, July 14, 2020 | Sheet 55 of 100

Vendor confirmed completion on 3/18



Audio Power (5V/1.8V)



C_{TX} (pF)	Rise Time (µs) 10%~90%, C_{LX}=0.1µF, C_{INX}=1µF, R_{OX}=10Ω Typical Values at 25°C, 25V X7R 10% Ceramic Cap.						
	V_{INX}=5V	3.3V	1.8V	1.5V	1.2V	1.05V	0.8V
0	85	68	49	45	40	37	34
220	431	297	172	147	122	106	89
470	888	583	332	269	218	189	161
1000	1700	1130	657	550	446	390	316
2200	3805	2534	1347	1152	966	867	701
4700	8053	5255	1997	2578	2101	1838	1483
10000	18330	12050	5545	5545	4155	4155	3329

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Issued Date	2020/10/01	Deciphered Date 2018/10/01	Title: P056 - Audio ALC3281
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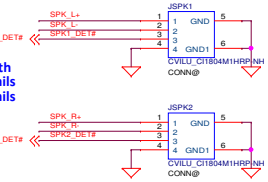
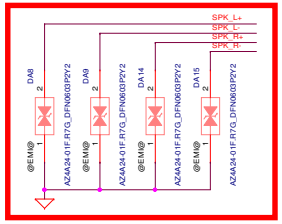
Vendor confirmed completion on 3/20

Int. Speaker Conn.

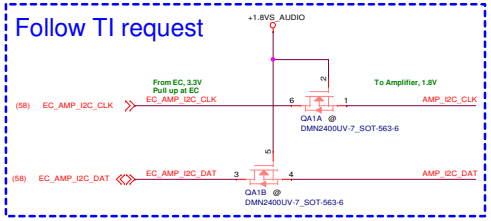
SPK L+ L- R+ R- trace width
Speaker 4 ohm ==> 40 mils
Speaker 8 ohm ==> 20 mils

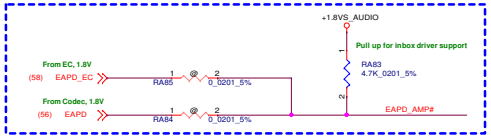


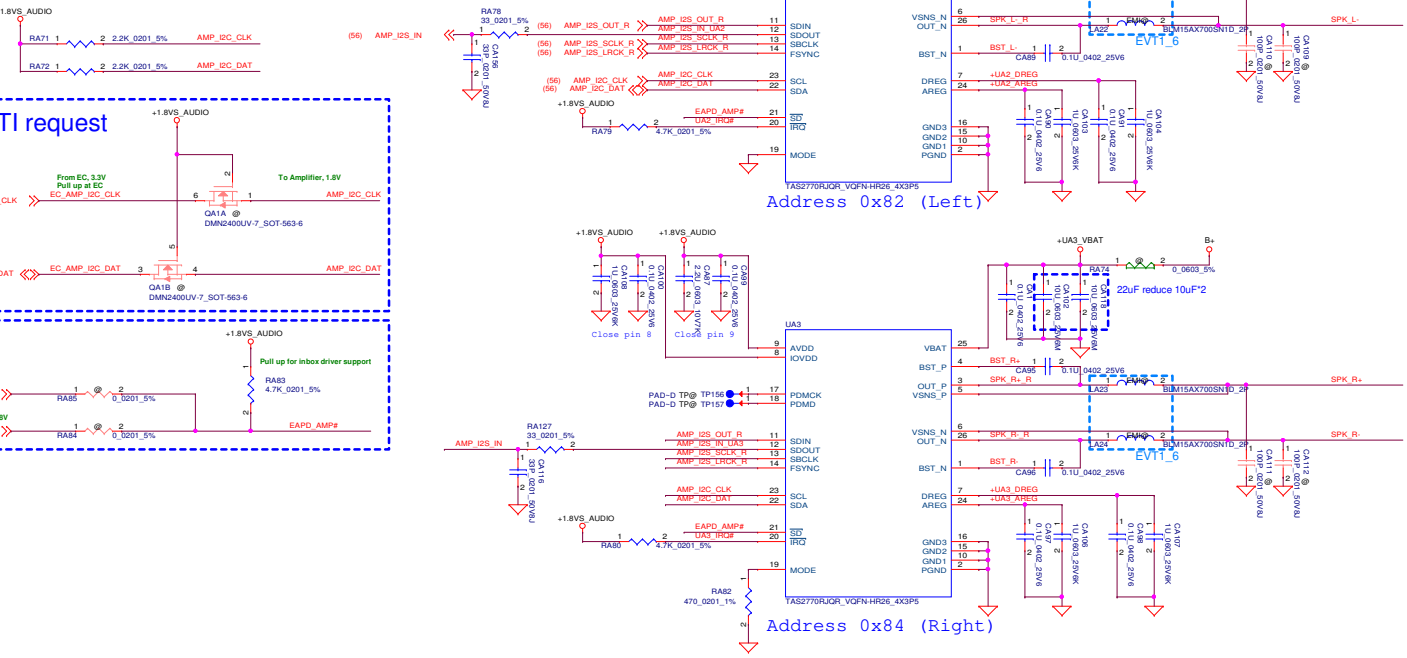


Need up to 15+V, check with EMC

Follow TI request



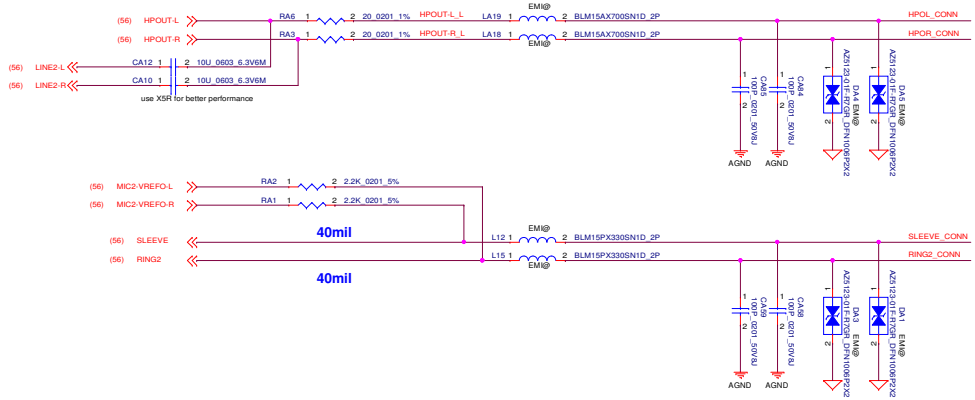




Universal Audio Jack

PCB trace width of MIC2-R(SLEEVE)/MIC2-L(RING2) are required at least 40 mil for HP crosstalk consideration and, its length should be as short as possible.
LA19/L15 should choose DC resistance (Rdc) < 30m-ohm to get the best audio performance for HP crosstalk.

change RA6/RA3 to 5.6 ohm to meet Dell Grade A headphone output power > 25 mW setting



Universal Audio Jack CONN

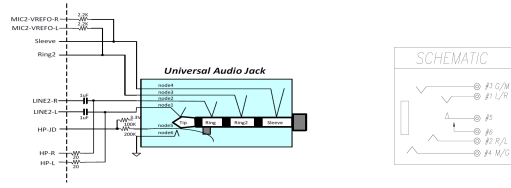
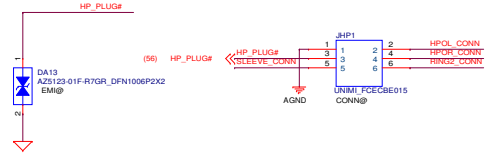


Figure 2. Analog Connector and Device

Contact with PC BEAN



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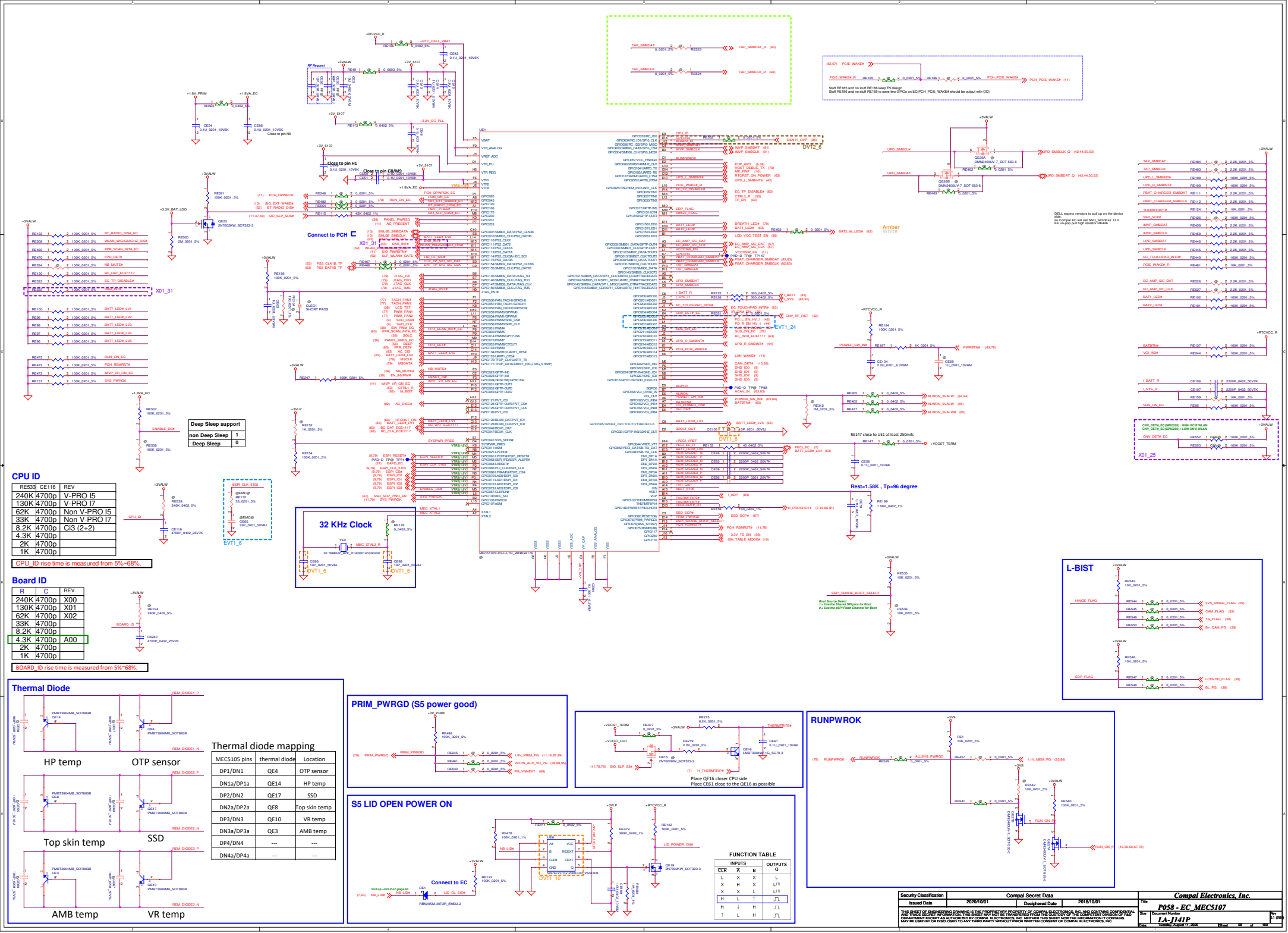
			Date: Tuesday, July 14, 2020; Sheet 57 of 100


CPU ID
RE533 CE116 REV
240K 4700p V-PRO I5
130K 4700p V-PRO I7
62K 4700p Non V-PRO I5
33K 4700p Non V-PRO I7
8.2K 4700p Ci3 (2+2)
4.3K 4700p
2K 4700p
1K 4700p
CPU_ID rise time is measured from 5%~68%.
Board ID
R C REV
240K 4700p X00
130K 4700p X01
62K 4700p X02
33K 4700p
8.2K 4700p
4.3K 4700p A00
2K 4700p
1K 4700p
BOARD_ID rise time is measured from 5%~68%.
Deep Sleep support
non Deep Sleep 1
Deep Sleep 0
32 KHz Clock
Thermal Diode
HP temp
OTP sensor
Top skin temp
SSD
AMB temp
VR temp
Thermal diode mapping
MEC5105 pins thermal diode Location
DP1/DN1 QE4 OTP sensor
DN1a/DP1a QE14 HP temp
DP2/DN2 QE17 SSD
DN2a/DP2a QE8 Top skin temp
DP3/DN3 QE10 VR temp
DN3a/DP3a QE3 AMB temp
DP4/DN4 --- ---
DN4a/DP4a --- ---
PRIM_PWRGD (S5 power good)
S5 LID OPEN POWER ON
FUNCTION TABLE
INPUTS OUTPUTS
CLR A B Q
L X X L
X H X L(1)
X X L L(1)
H L ↑ ⊥⊥
H ↓ H ⊥⊥
↑ L H ⊥⊥
RUNPWROK
L-BIST
Connect to PCH
Connect to EC
Amber White
Place QE16 closer CPU side
Place CE61 close to the QE16 as possible
Security Classification Compal Secret Data
Issued Date 2020/10/01 Deciphered Date 2018/10/01
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Title P058 - EC_MEC5107
Size Document Number LA-J141P Rev 1.1 (0D0)
Date: Tuesday, August 11, 2020 Sheet 58 of 100

Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

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Title: **P059 - Reserve**

Size	Document Number	Rev
	LA-J141P	0.1 (X00)

Date: Tuesday, July 14, 2020 | Sheet 59 of 100

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Title: **P060 - Reserve**

Size	Document Number	Rev
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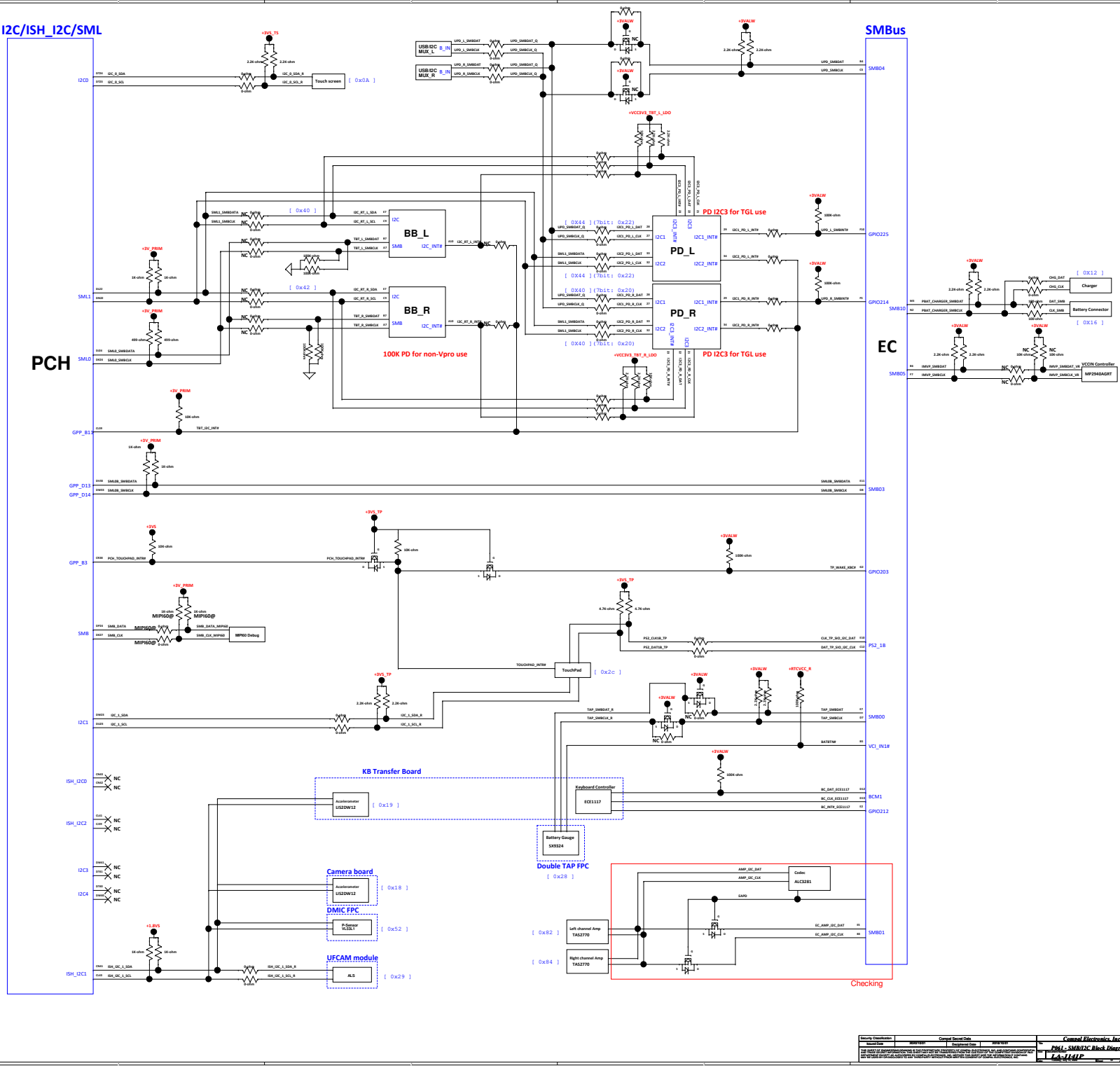
Date: Tuesday, July 14, 2020 | Sheet 60 of 100



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Issued Date	2020/10/01	Deciphered Date	2019/10/01	Title: P961 - SMB/I2C Block Diagram
			Size: LA-J141P	Doc Number: Rev: 1.0
			Date: Sheet: of	

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Title: **P062 - Reserve**

Size	Document Number	Rev
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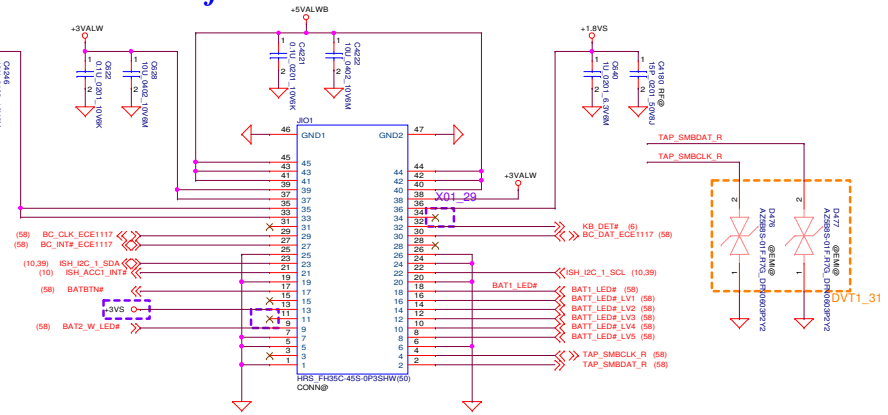
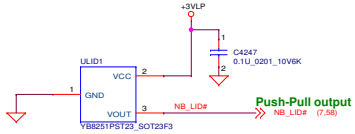
Date: Tuesday, July 14, 2020 | Sheet 62 of 100

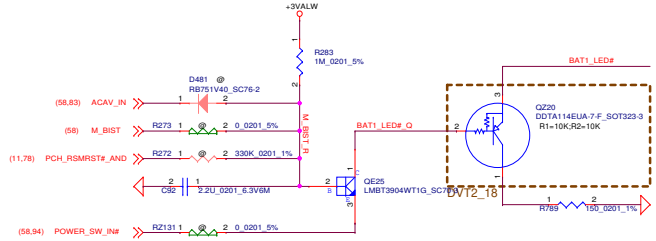
KB Controller & TP transfer Conn



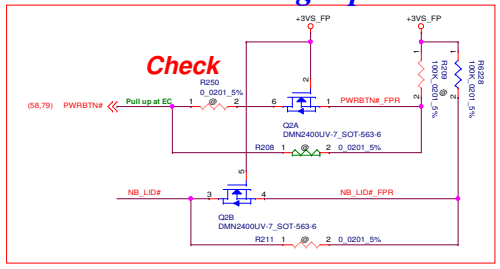
Hall sensor

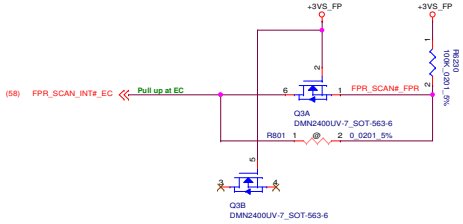


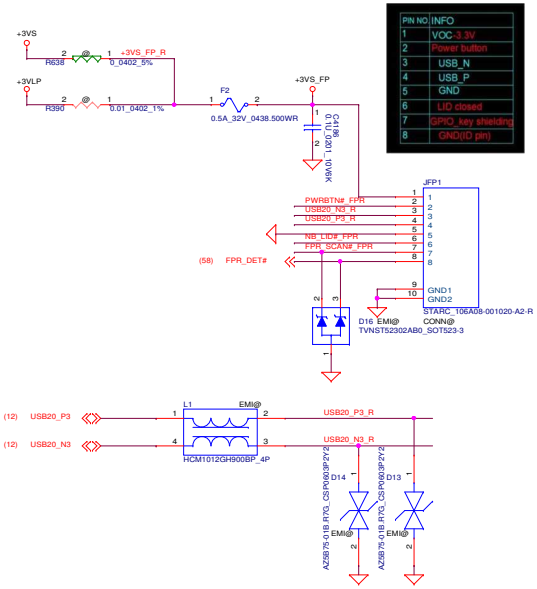
M-BIST



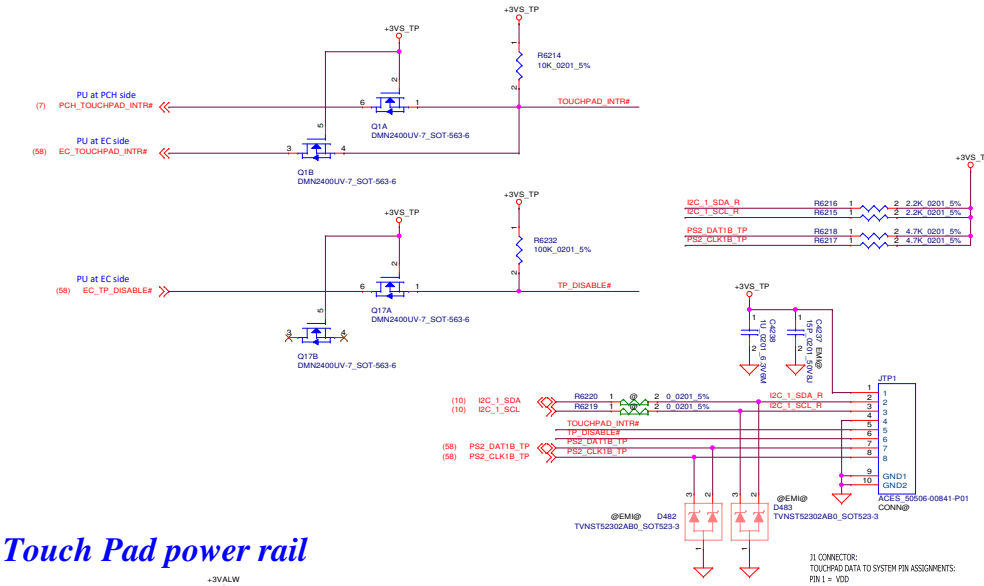
Power button & Finger print



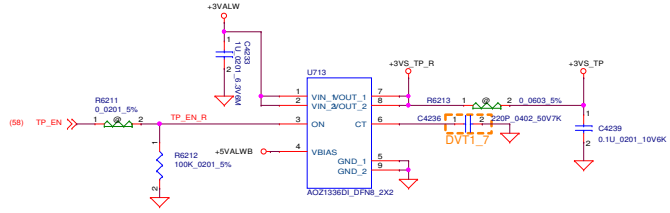




Touch PAD

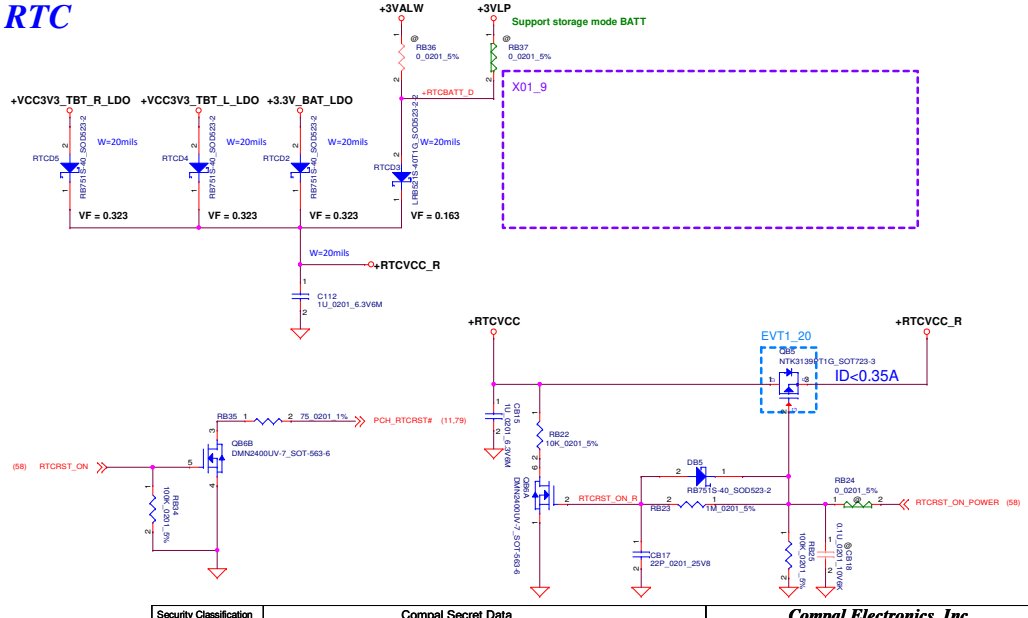


Touch Pad power rail



J1 CONNECTOR:
TOUCHPAD DATA TO SYSTEM PIN ASSIGNMENTS:
PIN 1 = VDD
PIN 2 = I2C DATA
PIN 3 = I2C CLK
PIN 4 = GND
PIN 5 = ATTN
PIN 6 = PTP DISABLE# (GPIO1,CLOSE LID)
PIN 7 = PS2 DATA
PIN 8 = PS2 CLK

RTC



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Title	P063 - KB/ TP/ FPR/ RTC
Size	Document Number: LA-J141P
Rev	0.1 (X00)
Date:	Tuesday, July 14, 2020
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Title: **P064 - Reserve**

Size	Document Number	Rev
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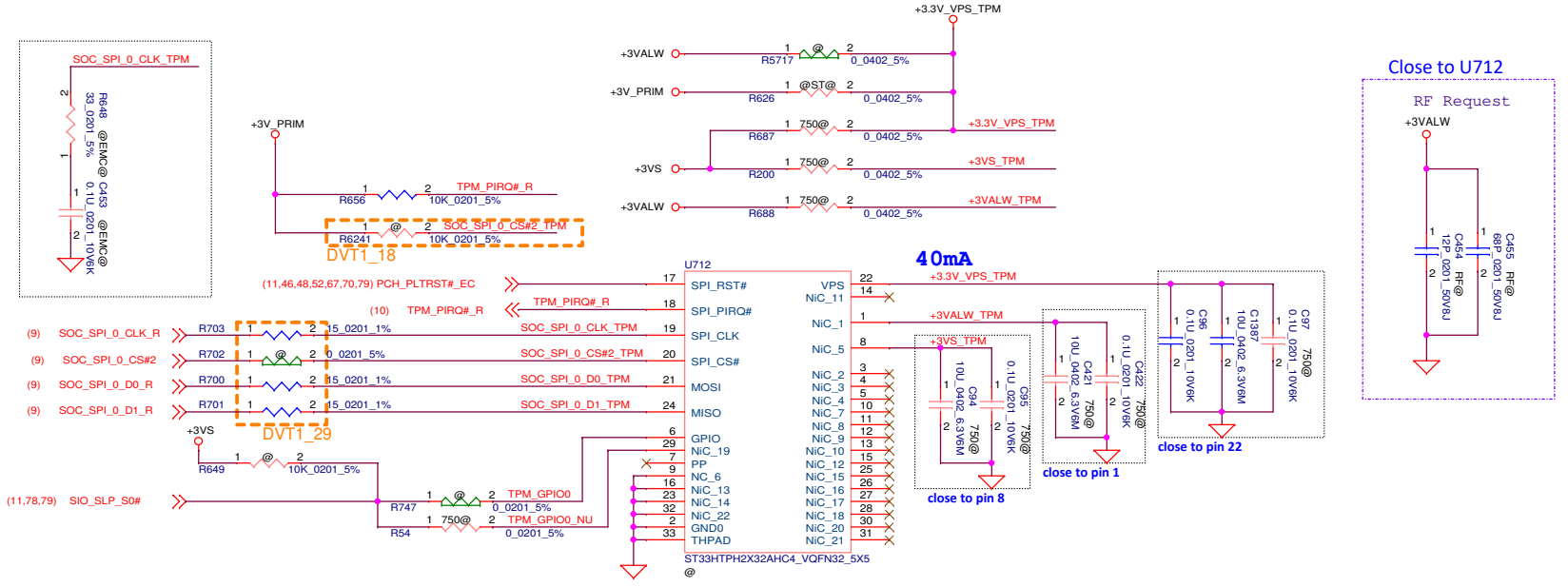
Title: **P065 - Reserve**

Size	Document Number	Rev
	LA-J141P	0.1 (X00)

Date: Tuesday, July 14, 2020 | Sheet 65 of 100

For ST/Nuvoton TPM



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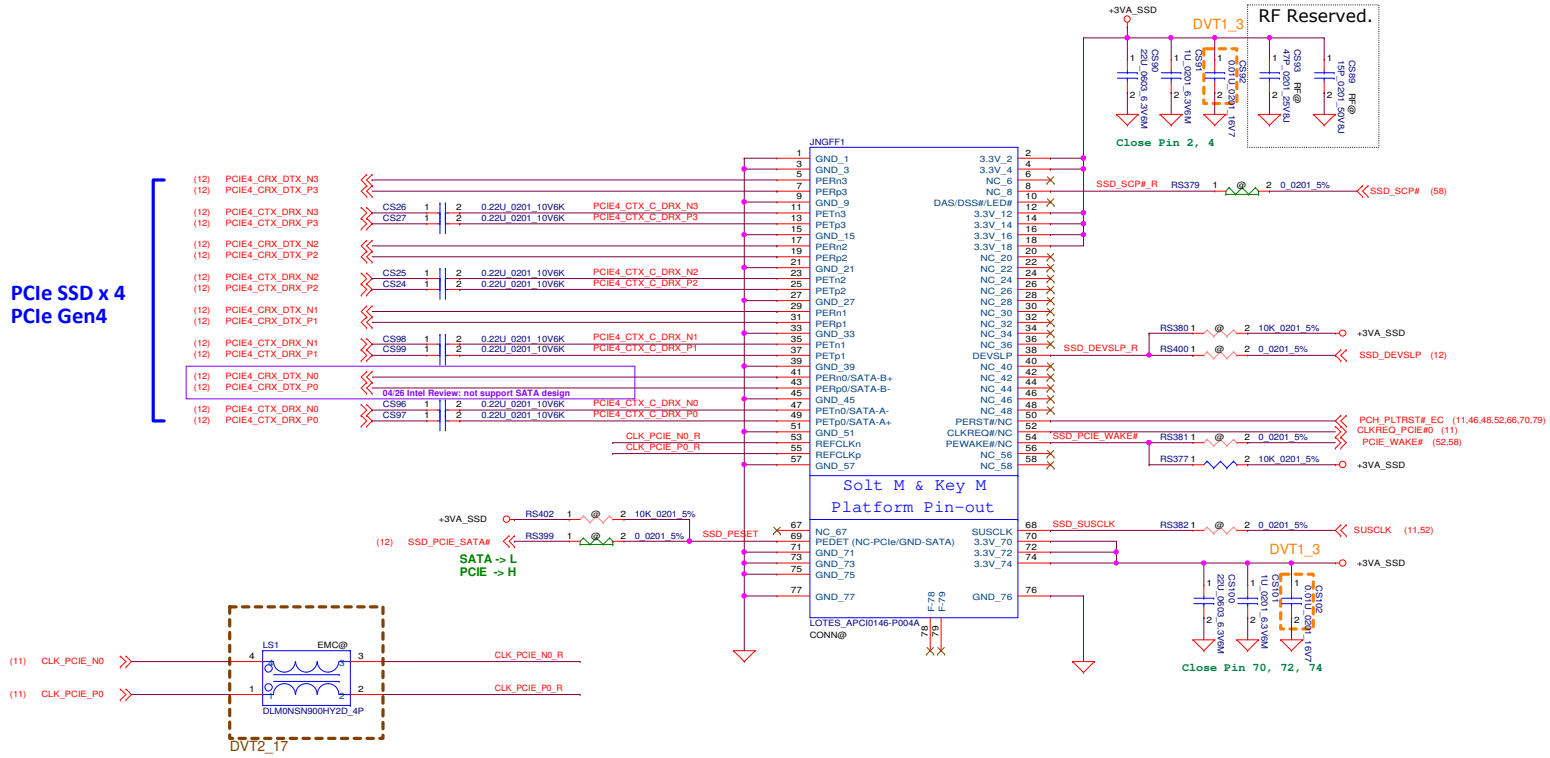
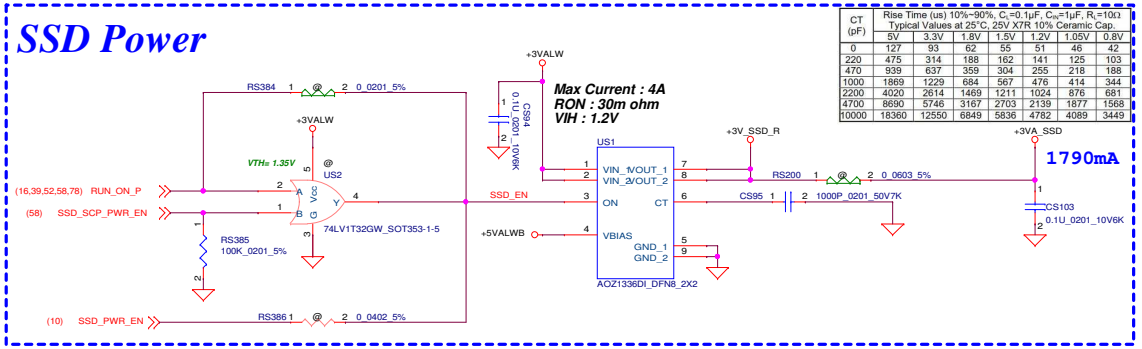
Compal Electronics, Inc.

Title: **P066 - TPM**

Size | Document Number: **LA-J141P** | Rev: 0.1 (X00)

Date: Tuesday, July 14, 2020 | Sheet 66 of 100





CT (pF)	Rise Time (us) 10%~90%, C_L=0.1µF, C_{PI}=1µF, R_L=10Ω Typical Values at 25°C, 25V X7R 10% Ceramic Cap.						
	5V	3.3V	1.8V	1.5V	1.2V	1.05V	0.8V
0	127	93	62	55	51	46	42
220	475	314	188	162	141	125	103
470	939	637	359	304	255	218	188
1000	1869	1229	684	567	476	414	344
2200	4020	2614	1469	1211	1024	876	681
4700	8690	5746	3167	2703	2139	1877	1568
10000	18360	12550	6849	5836	4782	4089	3449

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Title	P067 - M.2 SSD CONN
Size	Document Number: LA-J141P
Rev	0.1 (X00)
Date:	Tuesday, July 14, 2020
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X01_8

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Title: **P068 - Reserve**

Size	Document Number	Rev
	LA-J141P	0.1 (X00)

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Issued Date	2020/10/01	Deciphered Date	2018/10/01

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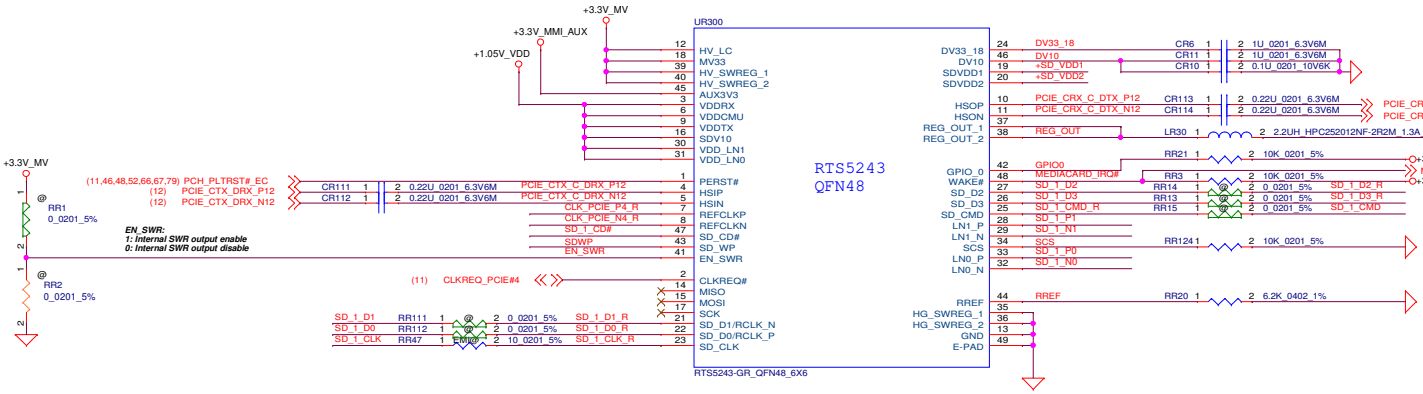
Title: **P069 - Reserve**

Size	Document Number	Rev
	LA-J141P	0.1 (X00)

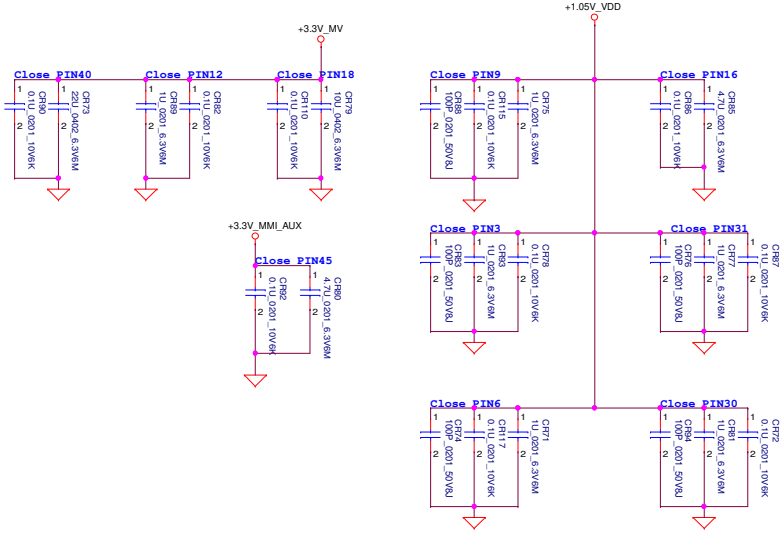
Date: Tuesday, July 14, 2020 | Sheet 69 of 100

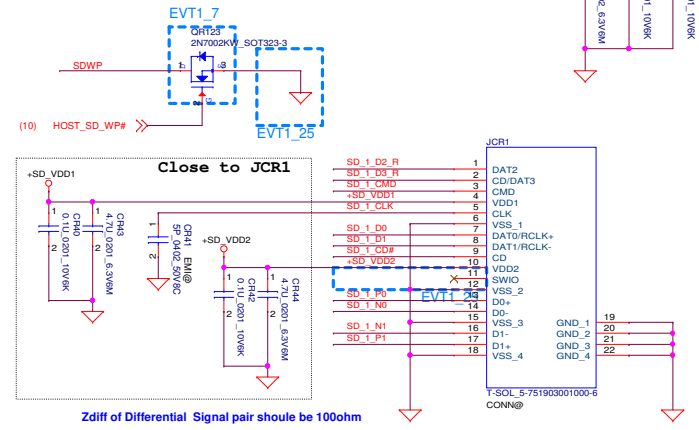
Vendor confirmed completion on 7/29

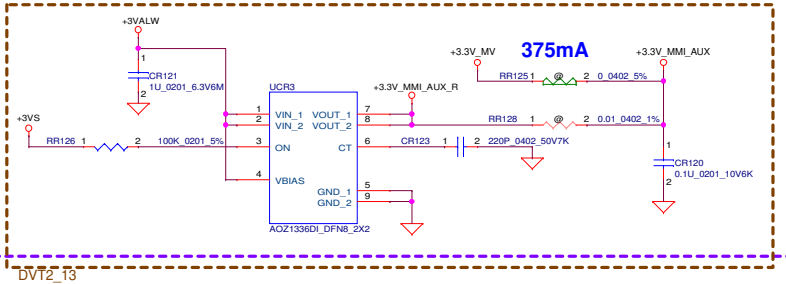
X01_17



X01:0610 Update RTS5243 Footprint

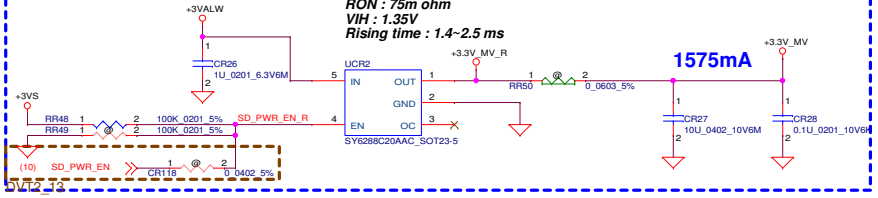






DVT2_13

Card Reader Power



DVT2_13

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Compal Electronics, Inc.	
Title	P070 - Card reader uSD RTS5243
Size	Document Number: LA-J141P
Rev	0.1 (X00)
Date: Tuesday, July 14, 2020	Sheet 70 of 100

Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

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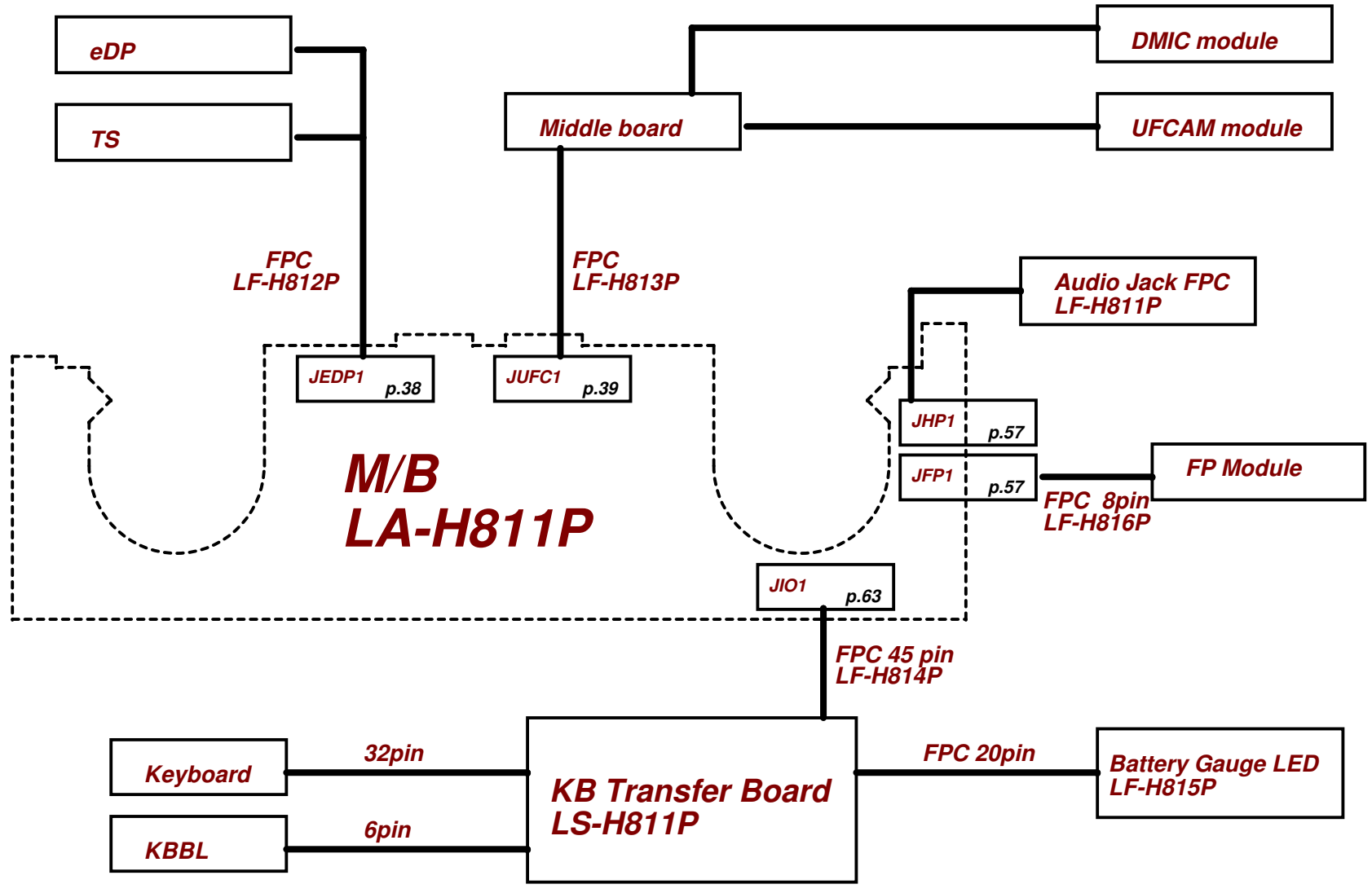
Compal Electronics, Inc.			
Title: P071 - Reserve			
Size	Document Number: LA-J141P		Rev: 0.1 (X00)
Date: Tuesday, July 14, 2020		Sheet 71 of 100	



Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

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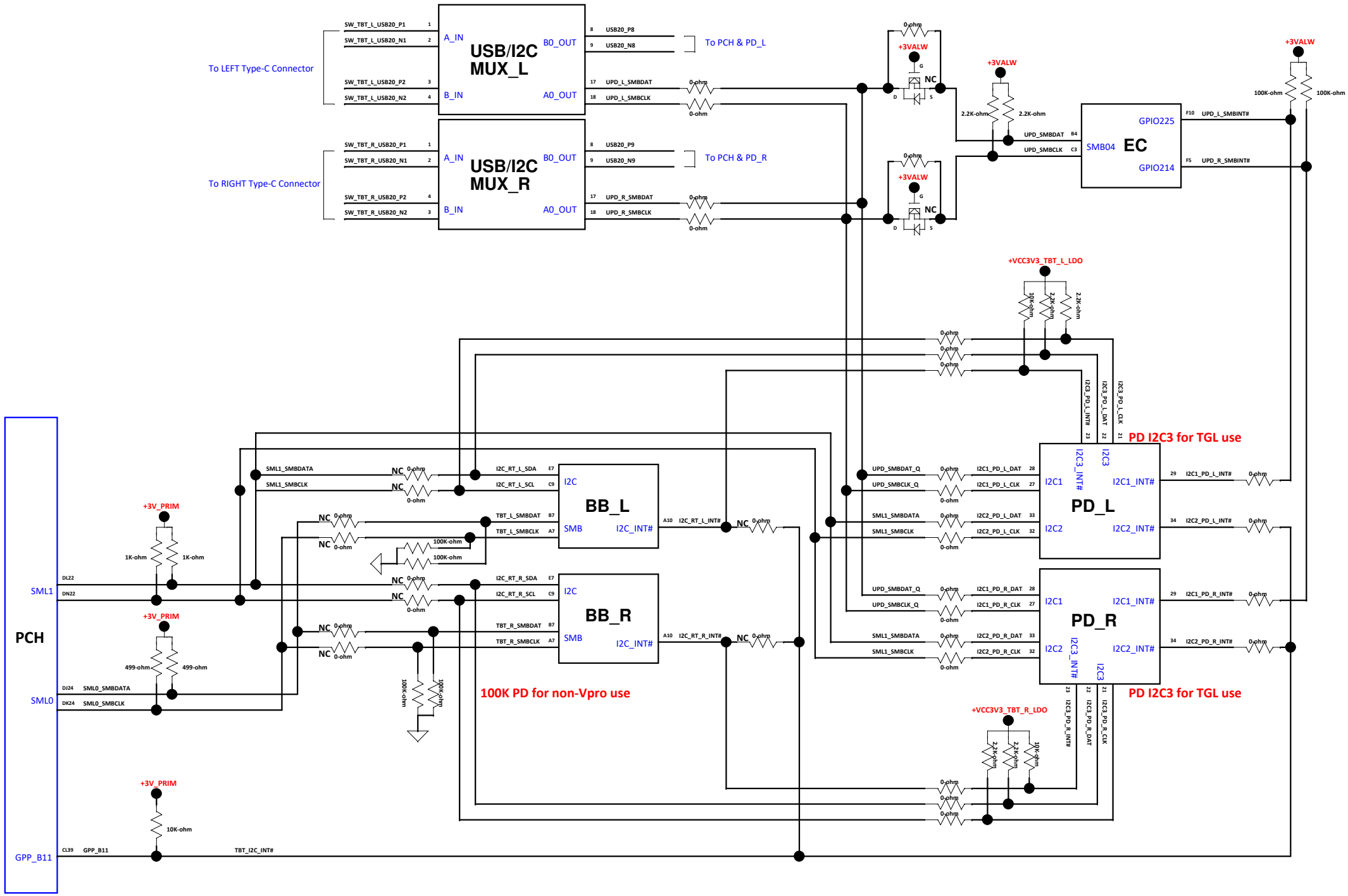
Compal Electronics, Inc.

Title: P072 - Board Map

Size | Document Number: LA-J141P | Rev: 0.1 (X00)

Date: Tuesday, July 14, 2020 | Sheet 72 of 100



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Issued Date	2020/10/01	Deciphered Date	2018/10/01

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Compal Electronics, Inc.

Title: P073 -TBT I2C/SML block diagram

Size: | Document Number: LA-J141P | Rev: 0.1 (X00)

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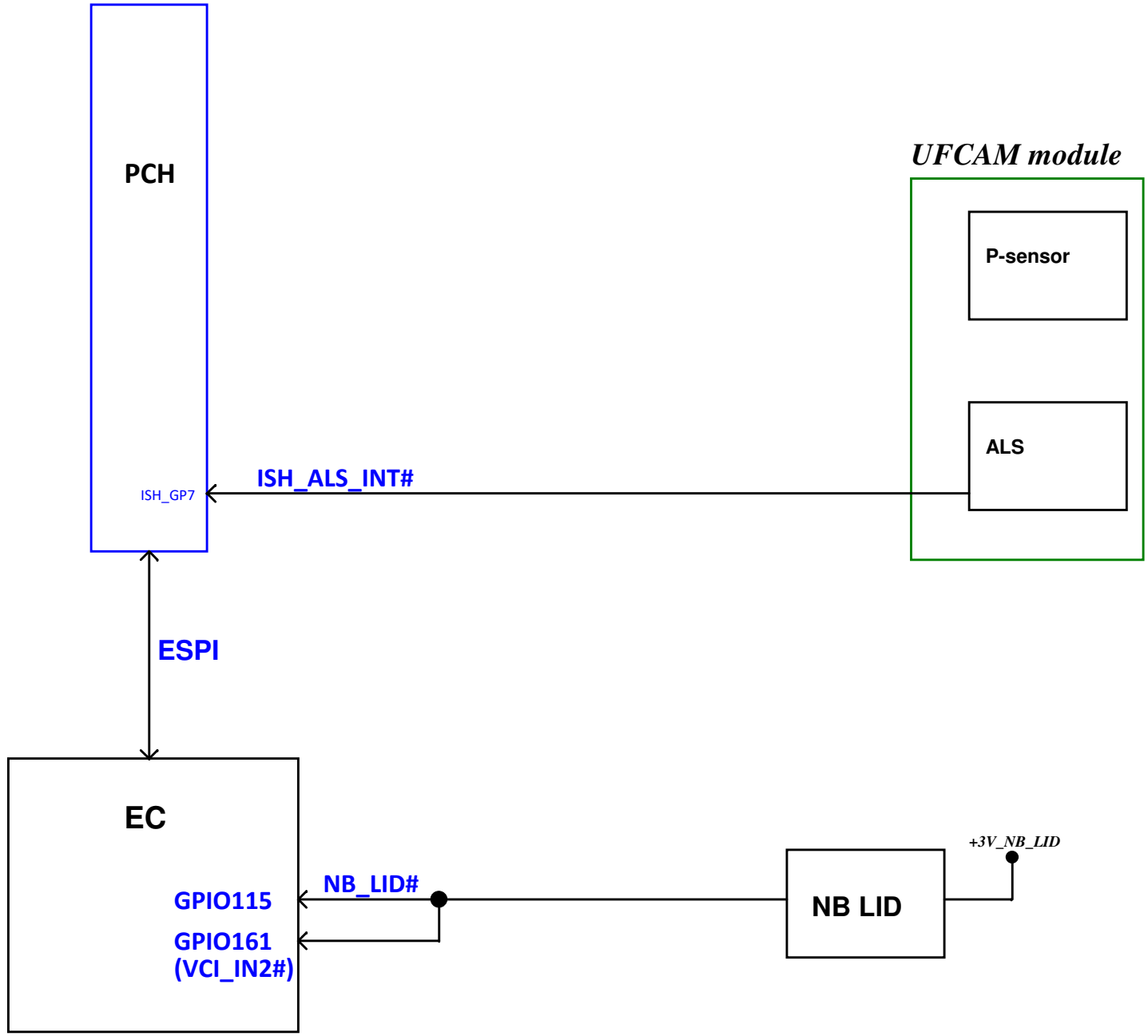

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Issued Date	2020/10/01	Deciphered Date	2018/10/01

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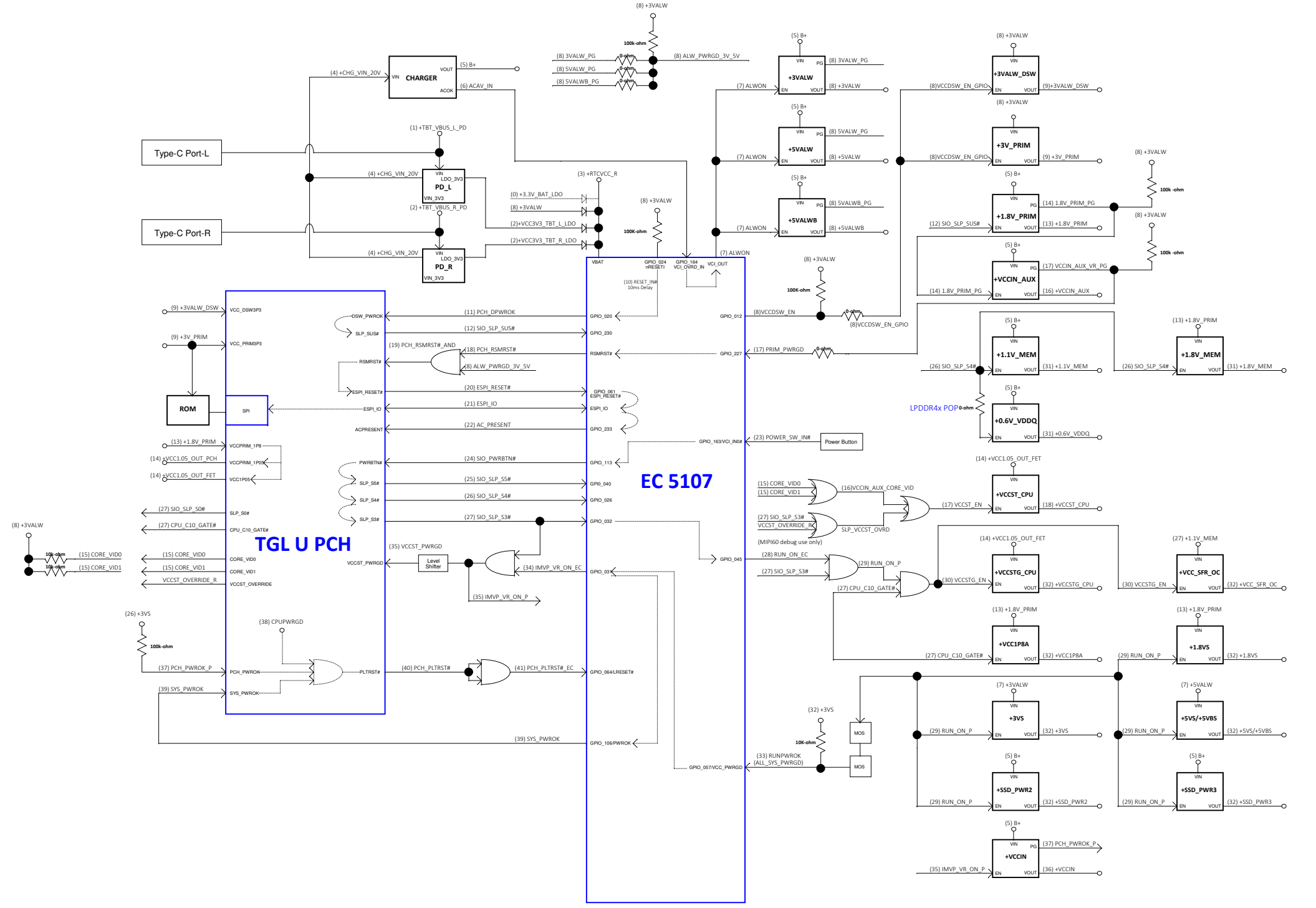
Compal Electronics, Inc.		
Title: P074 - Sensor block diagram		
Size	Document Number: LA-J141P	Rev: 0.1 (X00)
Date: Tuesday, July 14, 2020	Sheet 74 of 100	



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/10/01	Deciphered Date	2018/10/01	Title: P075 - AC_Power up Sequence
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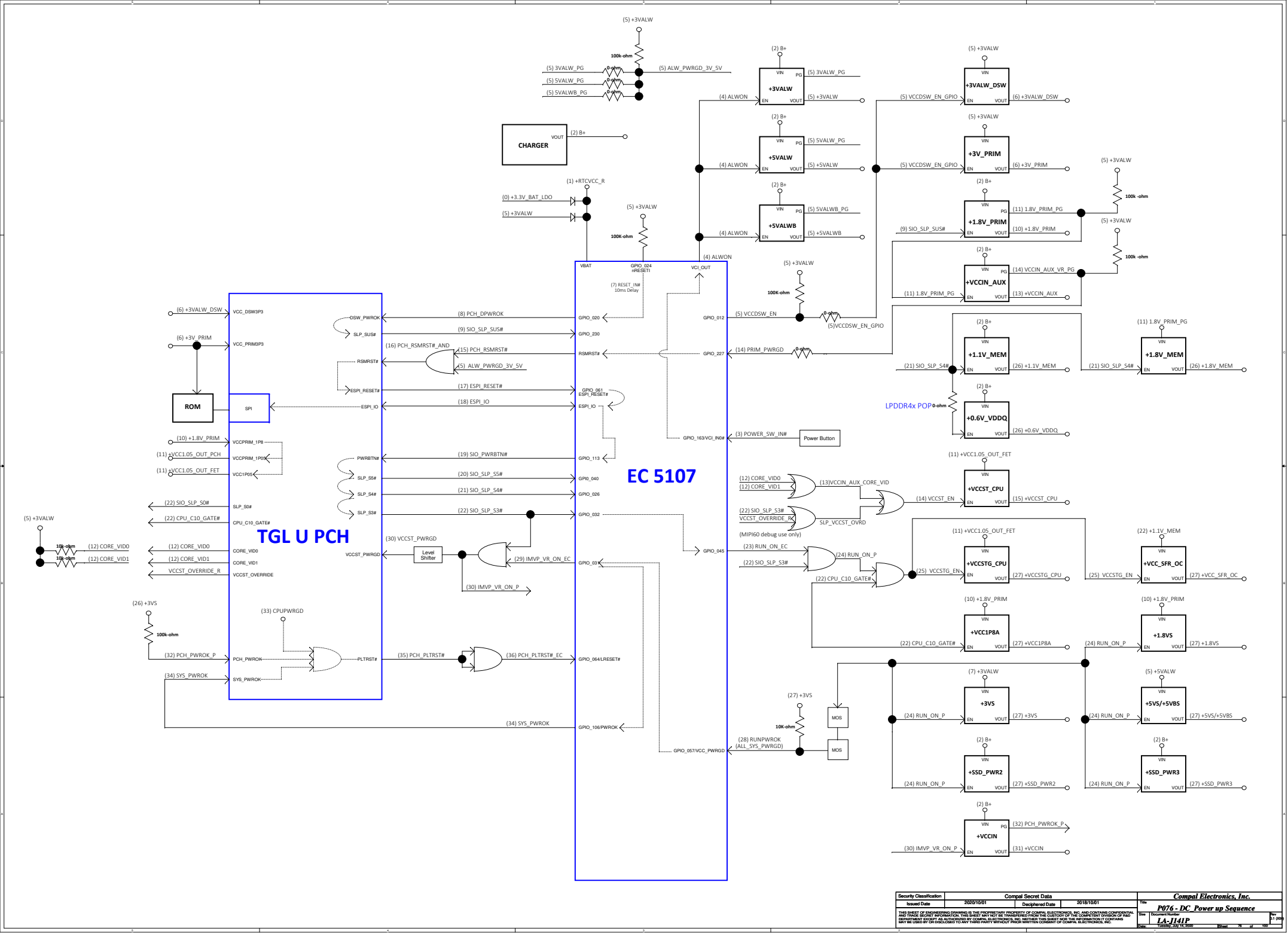
EC 5107
TGL U PCH
CHARGER
ROM
SPI
LPDDR4x POP
Power Button
Level Shifter
MOS
MOS
+3VALW
+5VALW
+5VALWB
+3VALW_DSW
+3V_PRIM
+1.8V_PRIM
+VCCIN_AUX
+1.1V_MEM
+0.6V_VDDQ
+1.8V_MEM
+VCCST_CPU
+VCCSTG_CPU
+VCC_SFR_OC
+VCC1P8A
+1.8VS
+3VS
+5VS/+5VBS
+SSD_PWR2
+SSD_PWR3
+VCCIN
(5) +3VALW
(2) B+
(1) +RTCVCC_R
(0) +3.3V_BAT_LDO
100k-ohm
0-ohm
(5) 3VALW_PG
(5) 5VALW_PG
(5) 5VALWB_PG
(5) ALW_PWRGD_3V_5V
(4) ALWON
(5) +5VALW
(5) +5VALWB
(5) VCCDSW_EN_GPIO
(6) +3VALW_DSW
(6) +3V_PRIM
(9) SIO_SLP_SUS#
(11) 1.8V_PRIM_PG
(10) +1.8V_PRIM
(14) VCCIN_AUX_VR_PG
(13) +VCCIN_AUX
(21) SIO_SLP_S4#
(26) +1.1V_MEM
(26) +1.8V_MEM
(26) +0.6V_VDDQ
(5) VCCDSW_EN
(5)VCCDSW_EN_GPIO
(14) PRIM_PWRGD
(3) POWER_SW_IN#
(11) +VCC1.05_OUT_FET
(12) CORE_VID0
(12) CORE_VID1
(13)VCCIN_AUX_CORE_VID
(22) SIO_SLP_S3#
VCCST_OVERRIDE_R
SLP_VCCST_OVRD
(MIPI60 debug use only)
(14) VCCST_EN
(15) +VCCST_CPU
(23) RUN_ON_EC
(24) RUN_ON_P
(22) CPU_C10_GATE#
(25) VCCSTG_EN
(27) +VCCSTG_CPU
(22) +1.1V_MEM
(27) +VCC_SFR_OC
(27) +VCC1P8A
(24) RUN_ON_P
(27) +1.8VS
(27) +3VS
(27) +5VS/+5VBS
(27) +SSD_PWR2
(27) +SSD_PWR3
(28) RUNPWROK
(ALL_SYS_PWRGD)
(32) PCH_PWROK_P
(31) +VCCIN
(30) IMVP_VR_ON_P
(7) RESET_IN# 10ms Delay
VBAT
GPIO_024 nRESET
VCI_OUT
GPIO_012
GPIO_227
GPIO_163/VCI_IN0#
GPIO_061 ESPI_RESET#
GPIO_020
GPIO_230
RSMRST#
ESPI_IO
GPIO_113
GPIO_040
GPIO_026
GPIO_032
GPIO_045
GPIO_03
GPIO_064/LRESET#
GPIO_106/PWROK
GPIO_057/VCC_PWRGD
VCC_DSW3P3
VCC_PRIM3P3
VCCPRIM_1P8
VCCPRIM_1P05
VCC1P05
SLP_S0#
CPU_C10_GATE#
CORE_VID0
CORE_VID1
VCCST_OVERRIDE
PCH_PWROK
SYS_PWROK
PLTRST#
DSW_PWROK
SLP_SUS#
RSMRST#
ESPI_RESET#
ESPI_IO
PWRBTN#
SLP_S5#
SLP_S4#
SLP_S3#
VCCST_PWRGD
CPUPWRGD
(8) PCH_DPWROK
(9) SIO_SLP_SUS#
(16) PCH_RSMRST#_AND
(15) PCH_RSMRST#
(17) ESPI_RESET#
(18) ESPI_IO
(19) SIO_PWRBTN#
(20) SIO_SLP_S5#
(21) SIO_SLP_S4#
(22) SIO_SLP_S3#
(29) IMVP_VR_ON_EC
(30) IMVP_VR_ON_P
(33) CPUPWRGD
(35) PCH_PLTRST#
(36) PCH_PLTRST#_EC
(34) SYS_PWROK
(22) SIO_SLP_S0#
(22) CPU_C10_GATE#
(12) CORE_VID0
(12) CORE_VID1
(10) +1.8V_PRIM
(11) +VCC1.05_OUT_PCH
(11) +VCC1.05_OUT_FET
(6) +3VALW_DSW
(6) +3V_PRIM
(26) +3VS
(34) SYS_PWROK
10K-ohm
Security Classification
Compal Secret Data
Issued Date
2020/10/01
Deciphered Date
2018/10/01
Compal Electronics, Inc.
P076 - DC_Power up Sequence
LA-J141P
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1.0
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Tuesday, July 14, 2020
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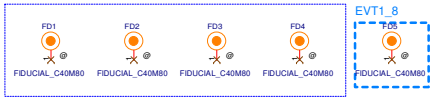
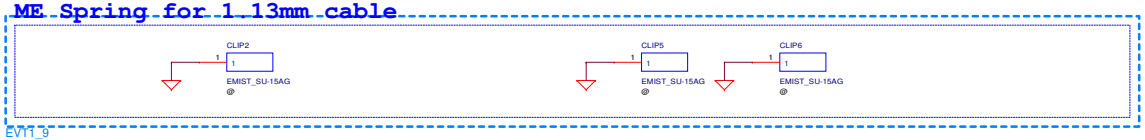
of
100

Screw Hole

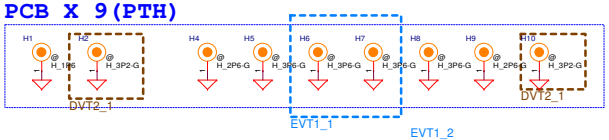
Fiducial Mark



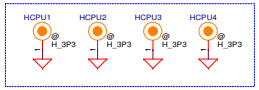
ME Spring for 1.13mm cable



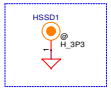
PCB X 9(PTH)



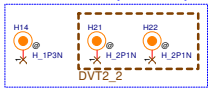
CPU X 4

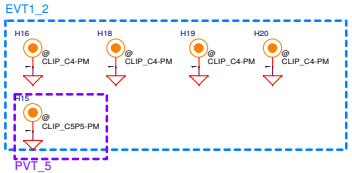


SSD stand-off



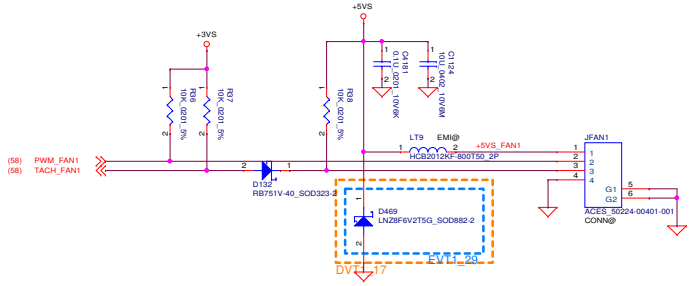
PCB X 3(NPTH)



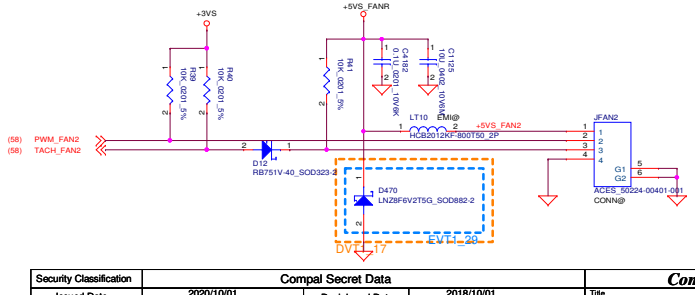


Positioning holes for CPU socket

FAN1



FAN2



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Issued Date	2020/10/01	Deciphered Date	2018/10/01

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Compal Electronics, Inc.			
Title	P077 - SCREW/ FAN		
Size	Document Number	LA-J141P	Rev 0.1 (X00)
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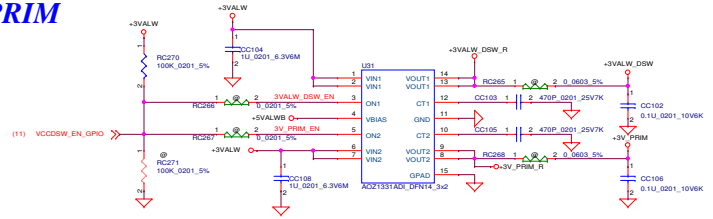
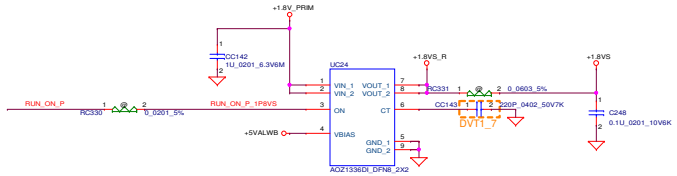
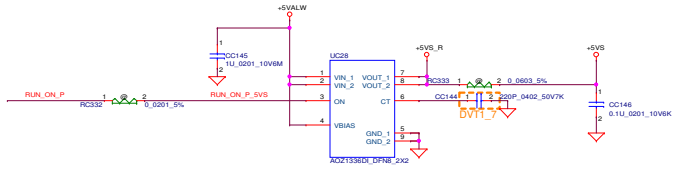
+3VALW_DSW
+3V_PRIM



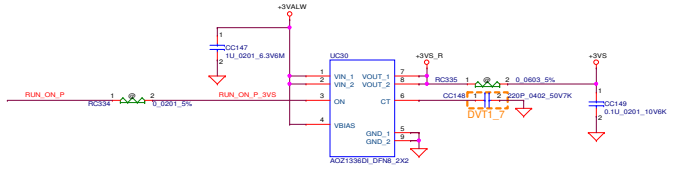
1.8VS



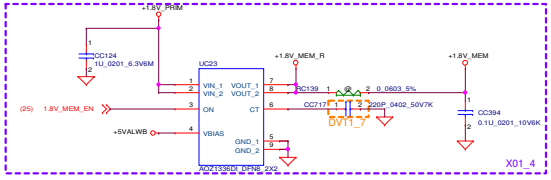
5VS



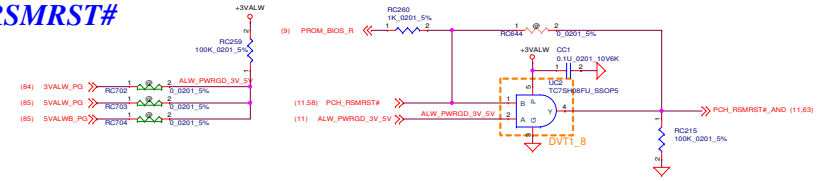
3VS



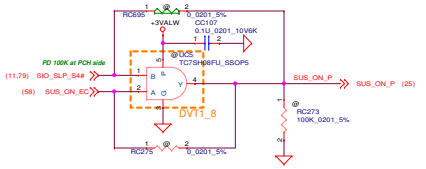
+1.8_MEM



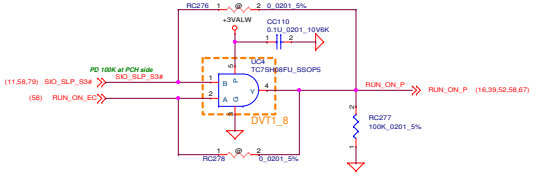
RSMRST#



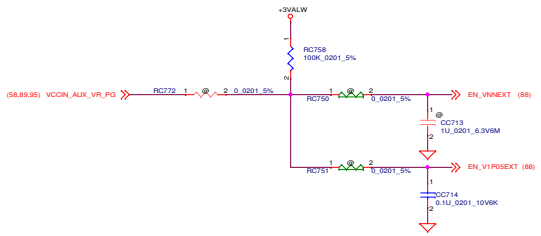
SUS_ON(DDR EN)



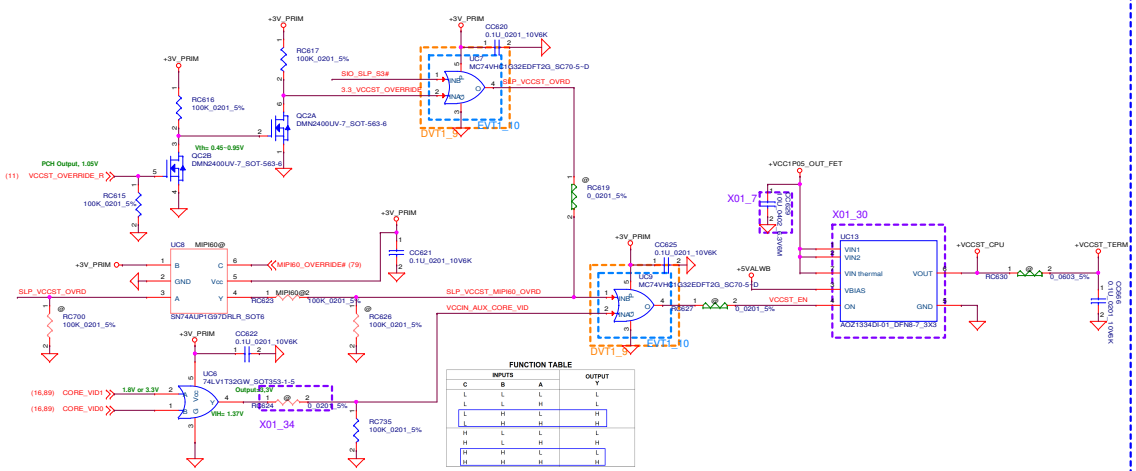
RUN_ON(VS EN)



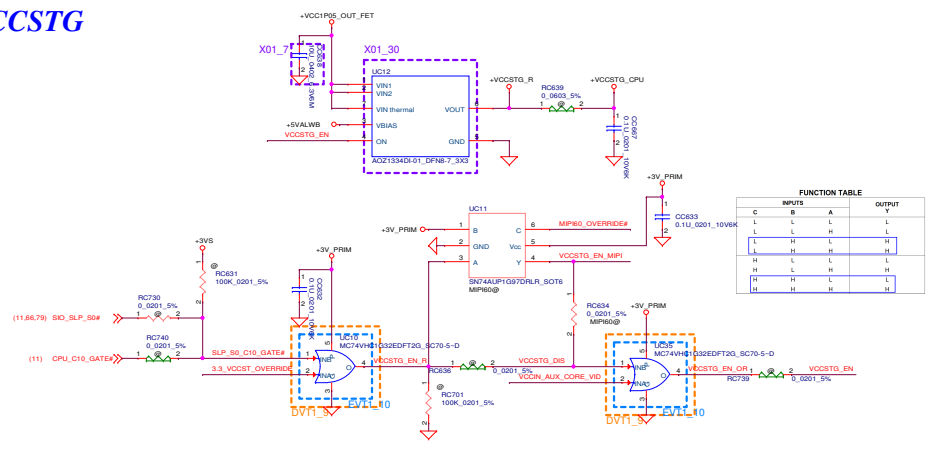
BYPASS Power Logic



VCCST



VCCSTG



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Issued Date	2020/10/01	Deciphered Date	2018/10/01

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Compal Electronics, Inc.			
Title: P078 - DC/DC & Sequence Logic			
Size	Document Number: LA-J141P		Rev: 0.1 (XD0)
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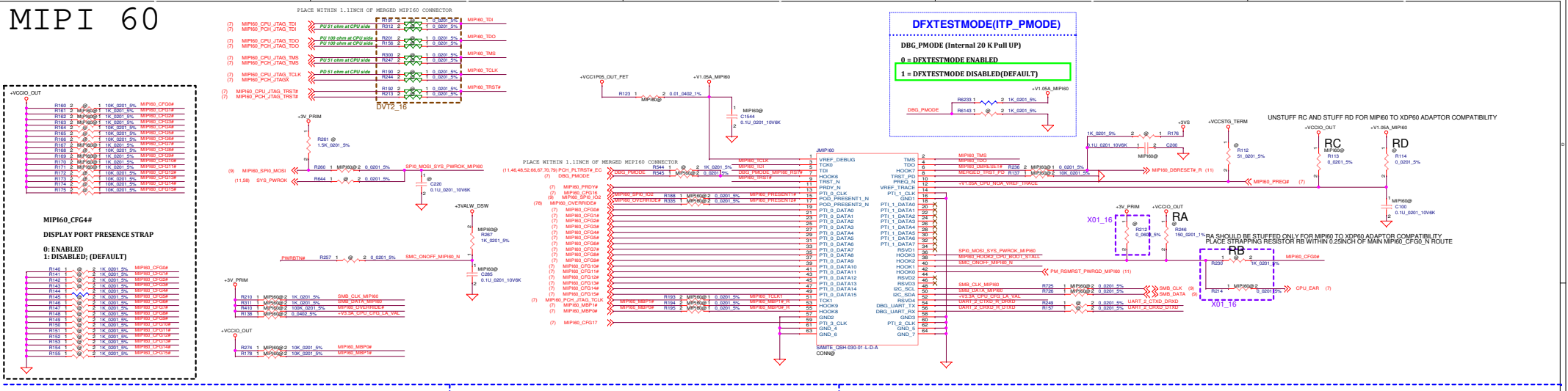
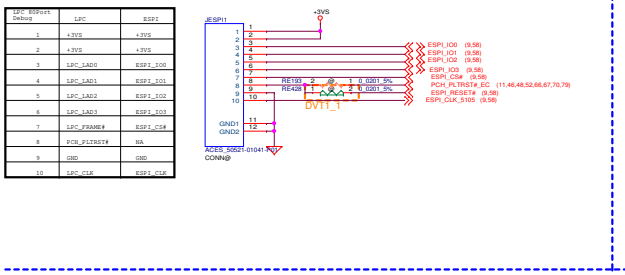
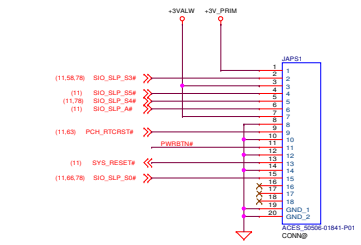
MIPI 60



JESPI

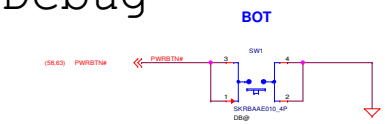


APS

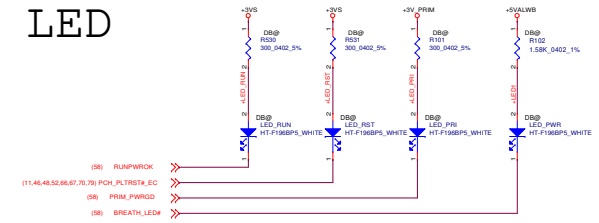


BIOS UART Debug

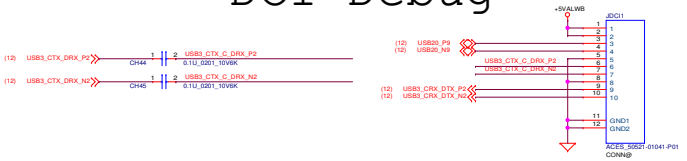
Power Button Debug



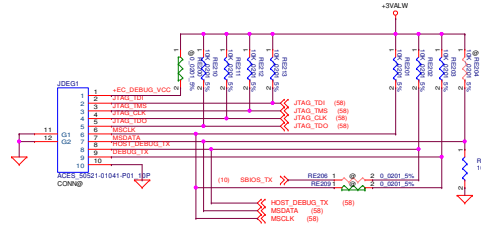
DEBUG LED



DCI Debug



JDEG1
EC UART Debug/80 port



Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

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Compal Electronics, Inc.	
Title	P079 - Debug APS,DEG,eSPI,LED
Size	Document Number: LA-J141P
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Security Classification	Compal Secret Data		
Issued Date	2020/10/01	Deciphered Date	2018/10/01

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Compal Electronics, Inc.

Title: **P080 - Reserved**

Size	Document Number	Rev
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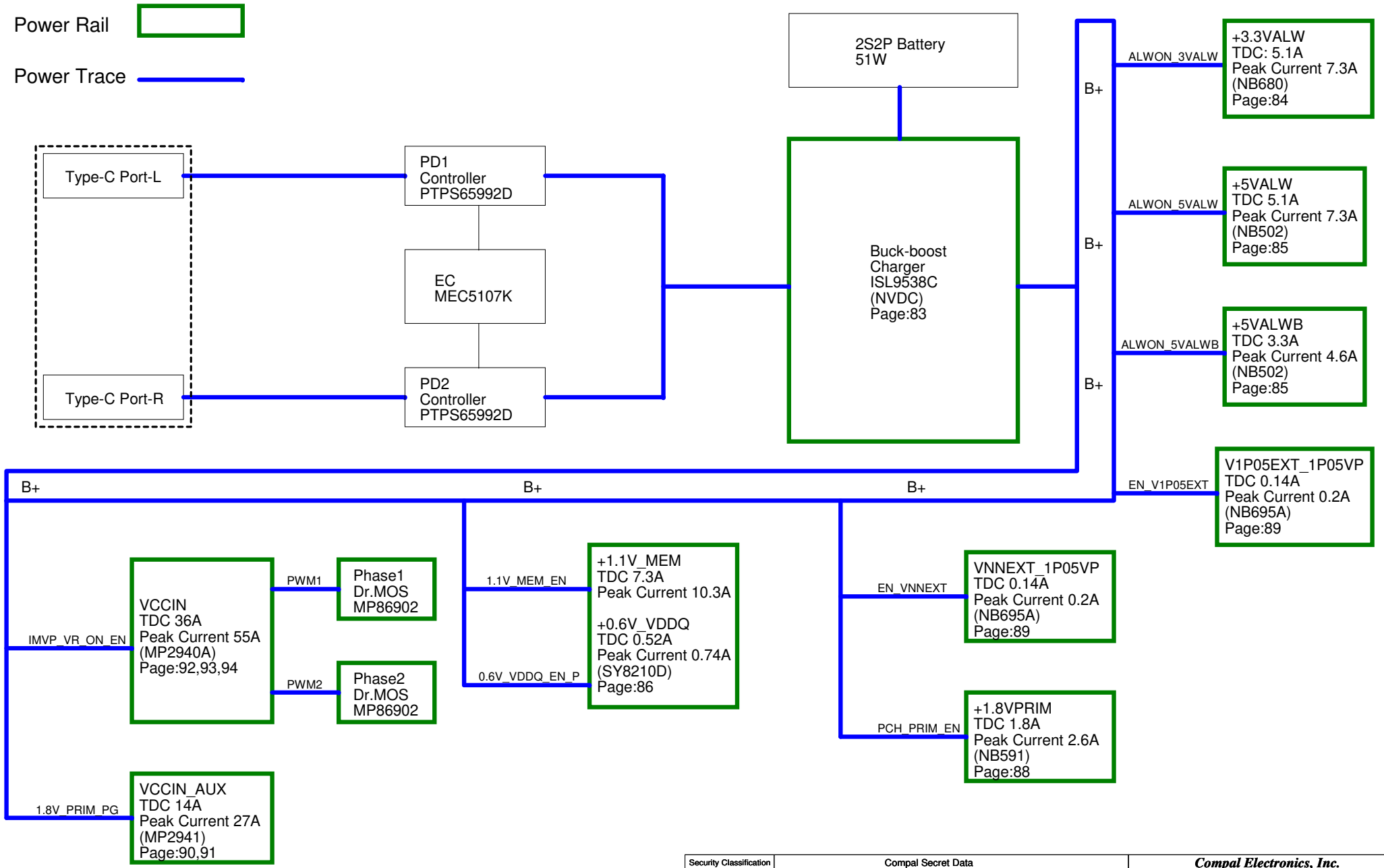
Modena MLK POWER BLOCK DIAGRAM



Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

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Compal Electronics, Inc.			
Title	PWR_POWER BLOCK DIAGRAM		
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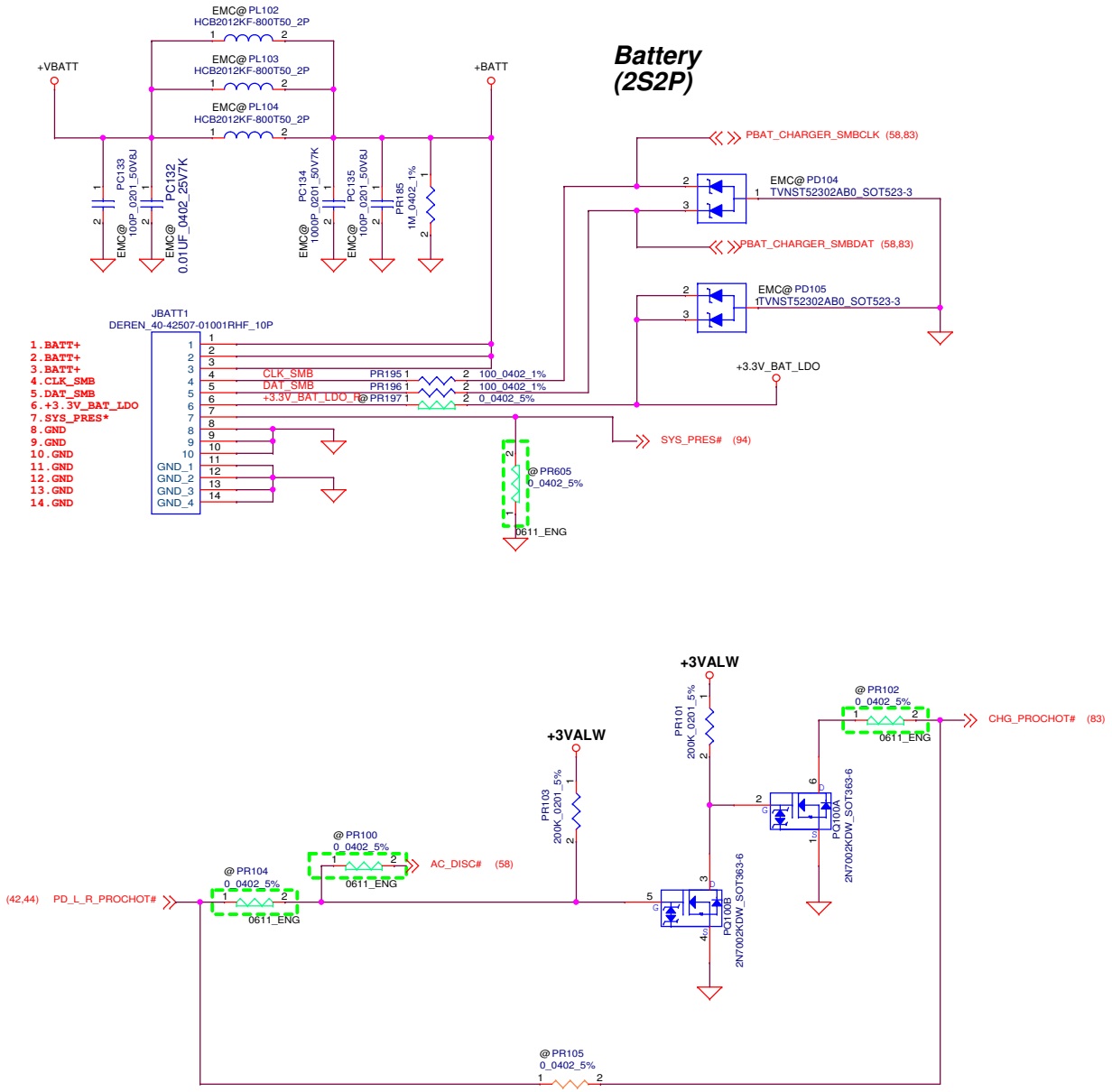
DCIN(37.1)



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Issued Date	2017/08/24	Deciphered Date	2017/08/24

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Compal Electronics, Inc.

Title: PWR DCIN

Size | Document Number: LA-J141P | Rev: 0.4 (X02)

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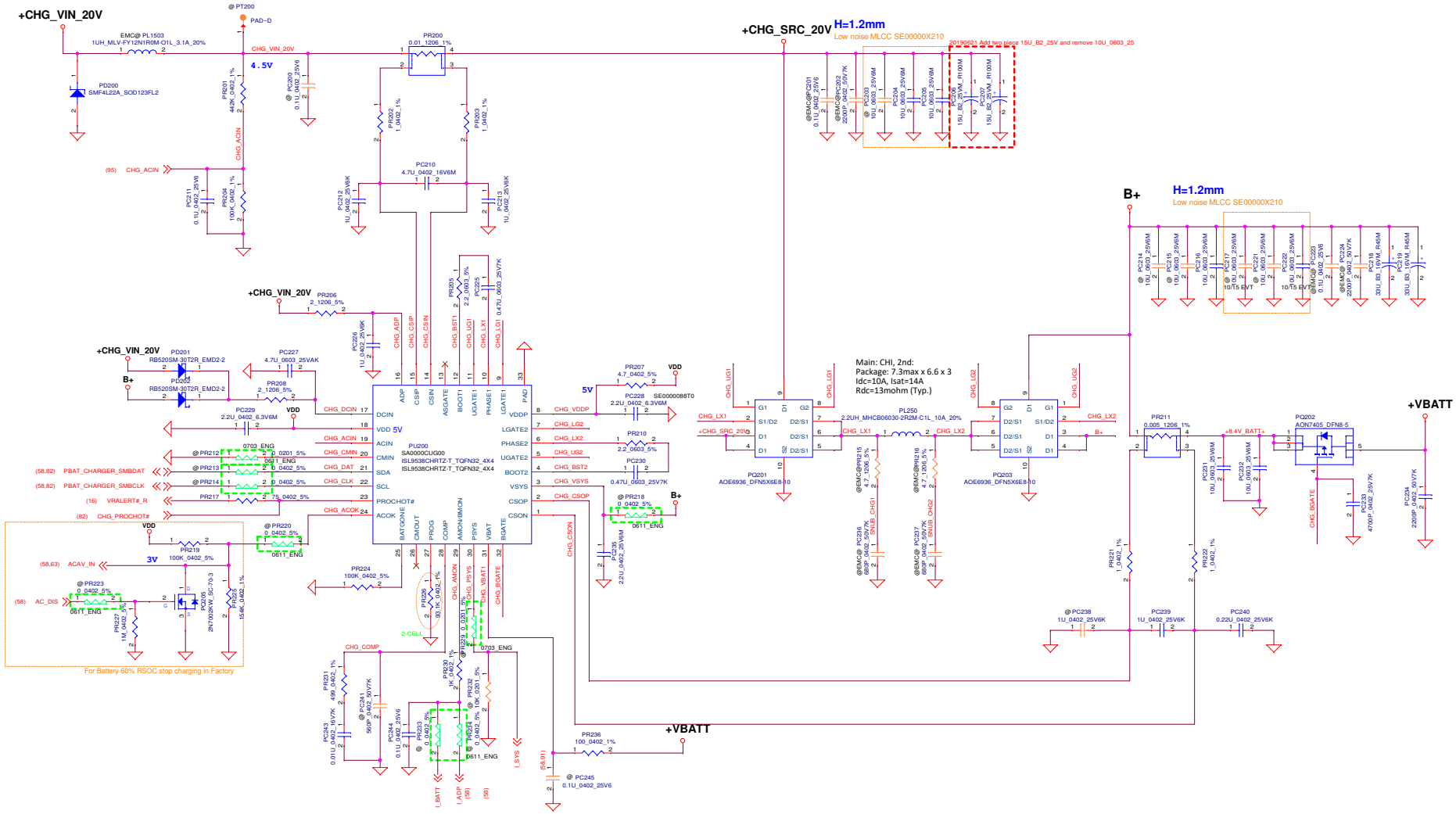
Charger controller(40.1), Support component(40.2)



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Compal Electronics, Inc.

Title: PWR_Charger

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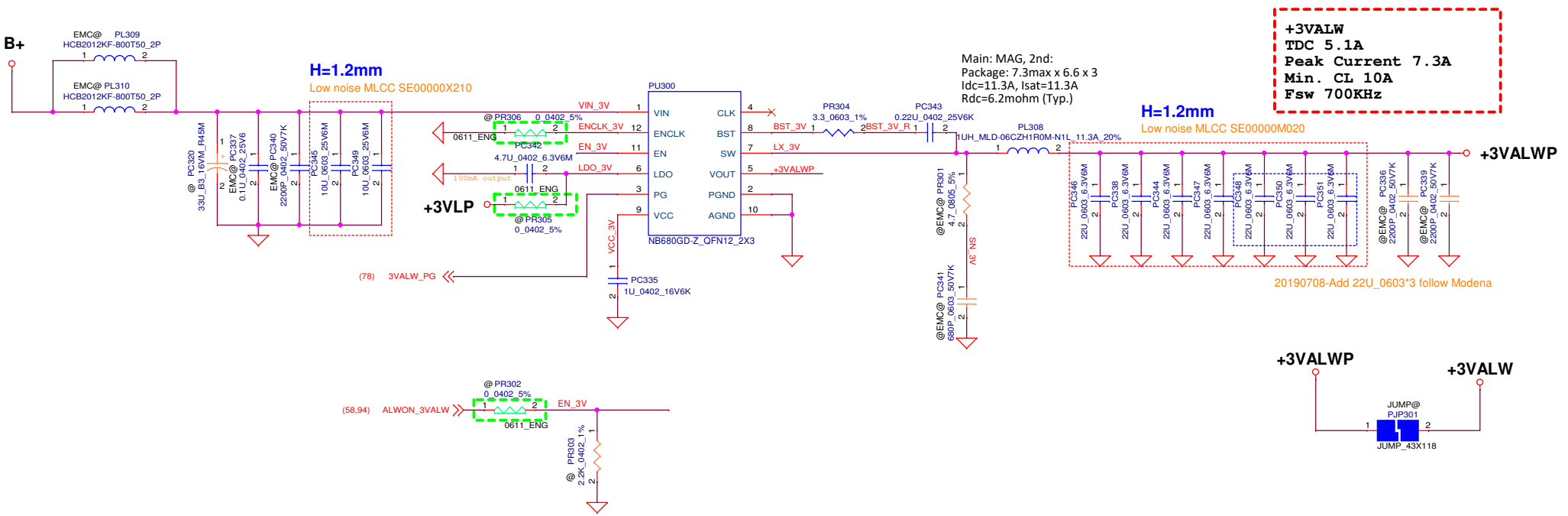
Controller(35.1), Support component(35.2)



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Compal Electronics, Inc.

Title: PWR +3VALW

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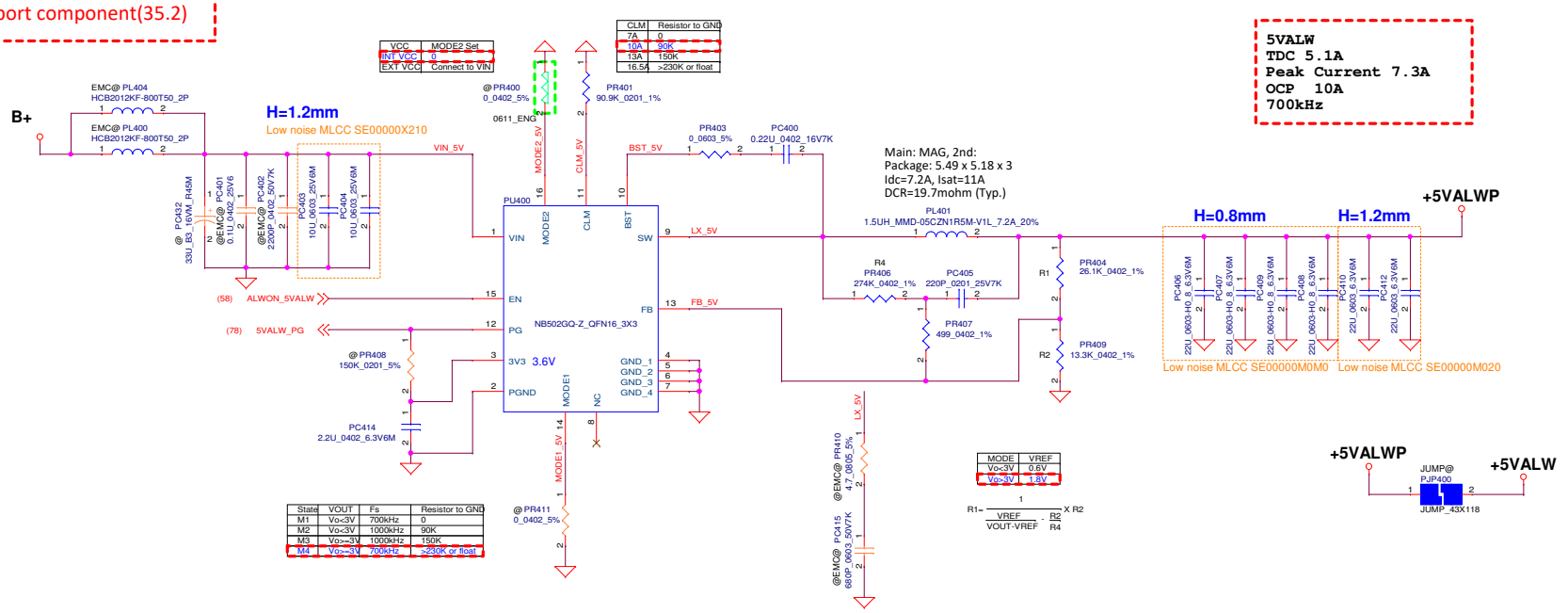
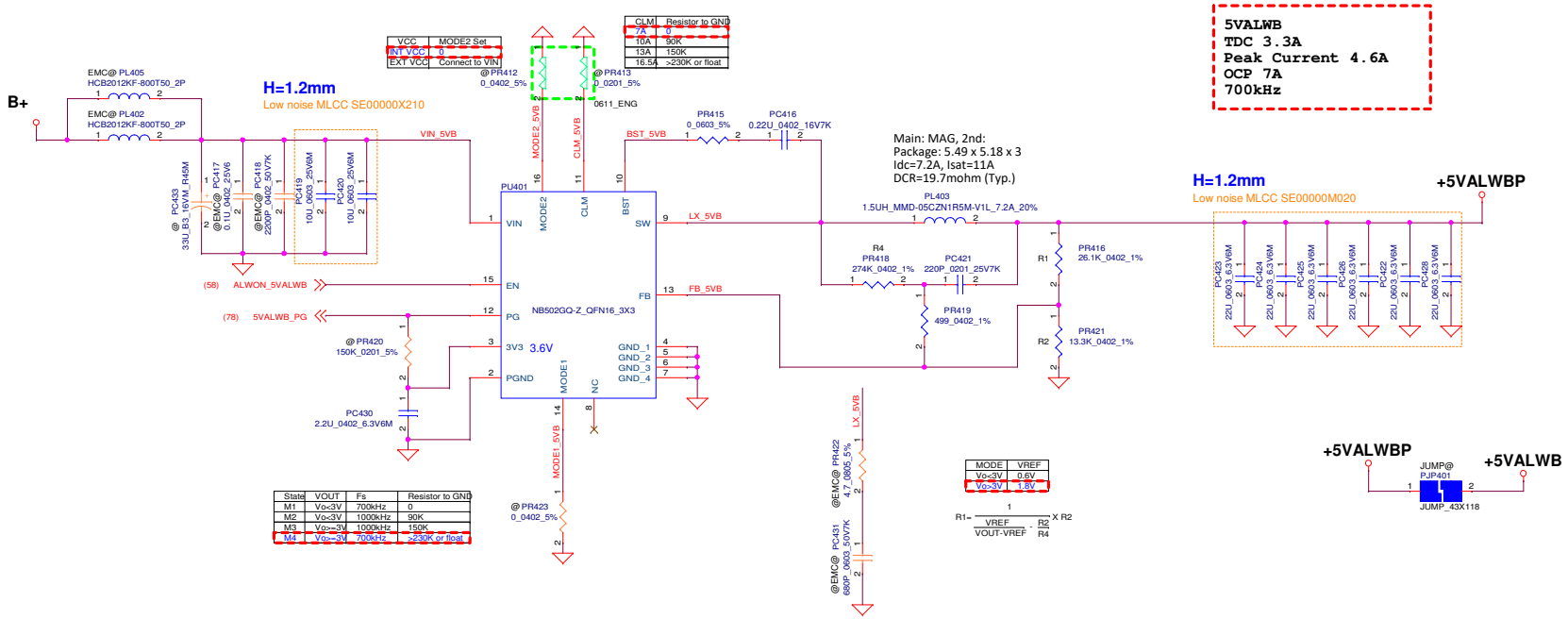
Controller(35.1), Support component(35.2)





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Compal Electronics, Inc.

Title: PWR_+5VALW/+5VALWB

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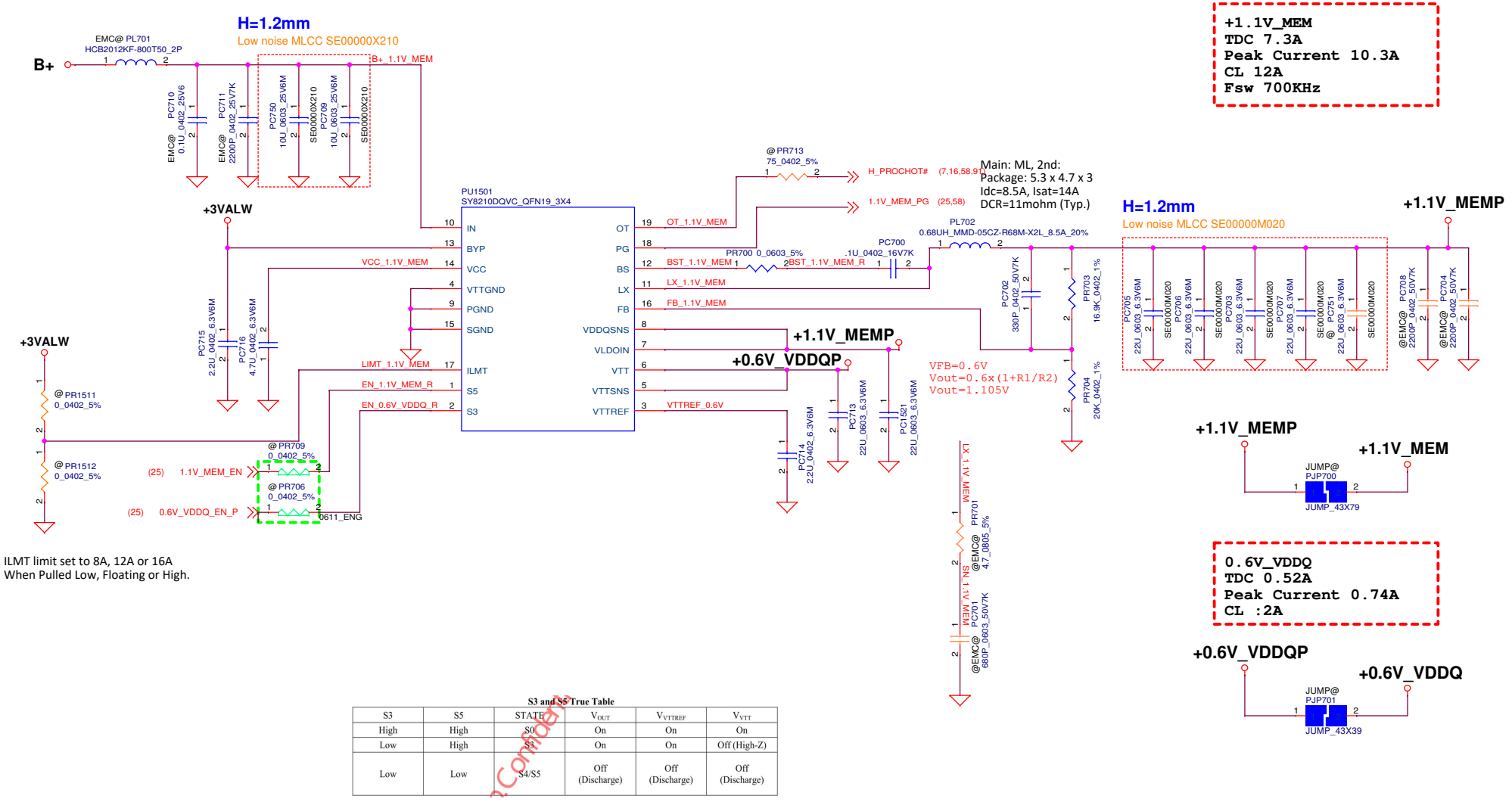
Controller(35.3), Support component(35.4)



+1.1V_MEM
TDC 7.3A
Peak Current 10.3A
CL 12A
Fsw 700KHz

0.6V_VDDQ
TDC 0.52A
Peak Current 0.74A
CL :2A

ILMT limit set to 8A, 12A or 16A
When Pulled Low, Floating or High.

S3 and S5 True Table

S3	S5	STATE	V_{OUT}	V_{VTTREF}	V_{VTT}
High	High	S0	On	On	On
Low	High	S3	On	On	Off (High-Z)
Low	Low	S4/S5	Off (Discharge)	Off (Discharge)	Off (Discharge)

Compal

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Compal Electronics, Inc.

Title: PWR_+1.1V_MEM/+0.6_VDDQ

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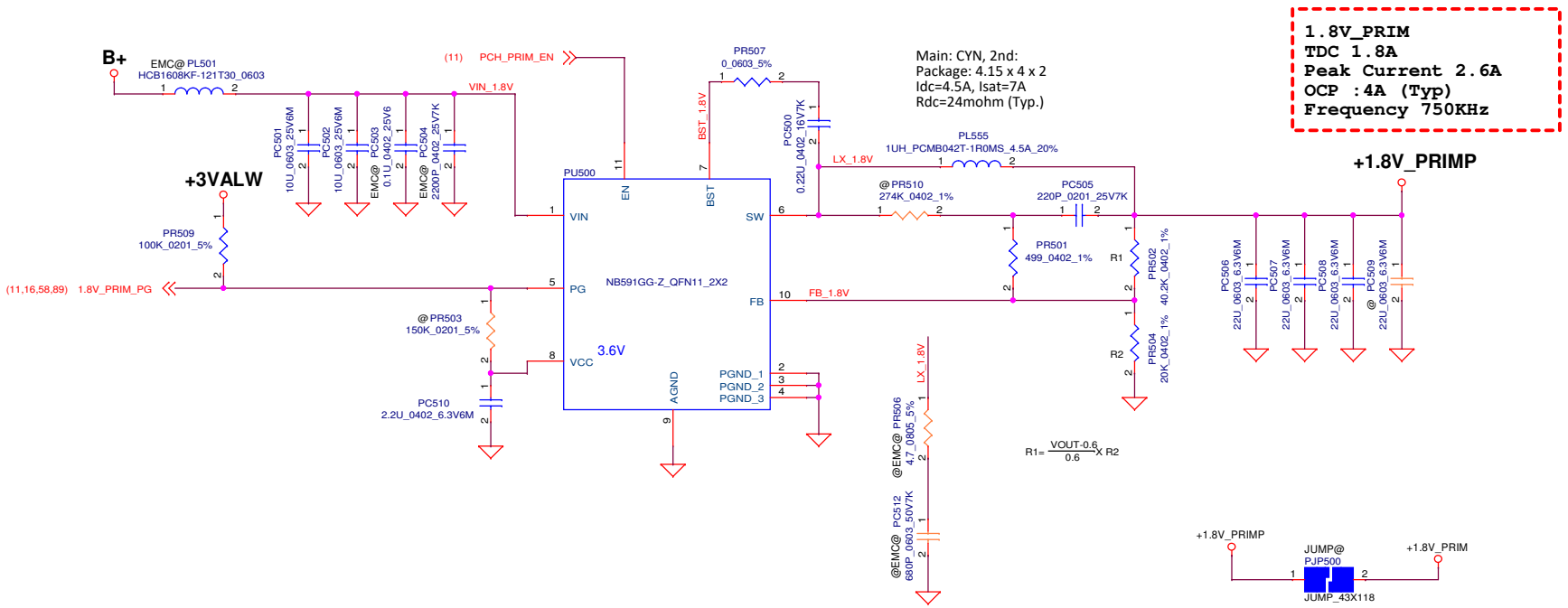
Controller(35.13), Support component(35.14)



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Compal Electronics, Inc.

Title: PWR_+1.8VPRIM

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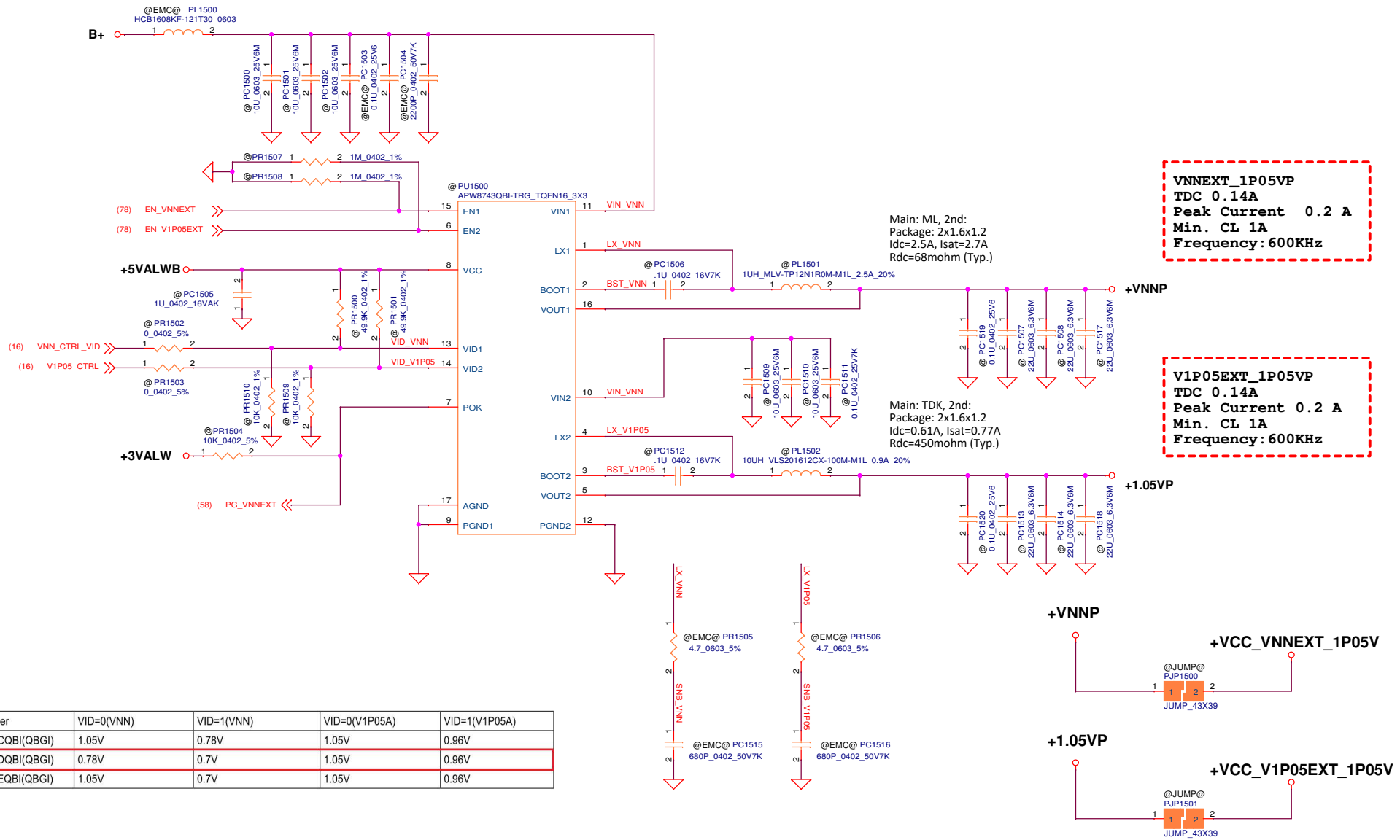
VNN and 1.05 Bypass (Intel) controller(35.33), Support component(35.34)



Part Number	VID=0(VNN)	VID=1(VNN)	VID=0(V1P05A)	VID=1(V1P05A)
APW8743CQBI(QBGI)	1.05V	0.78V	1.05V	0.96V
APW8743DQBI(QBGI)	0.78V	0.7V	1.05V	0.96V
APW8743EQBI(QBGI)	1.05V	0.7V	1.05V	0.96V

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Controller(36.1), Support component(36.3)

VCCIN_AUX (Base on ICL PDG rev 1.35)
Peak Current 27A (ICCmax)
TDC :14A
DC Load line :TBD mV/A
AC Load line :TBD mV/A
OCP Current 32A
Fsw=1000KHz

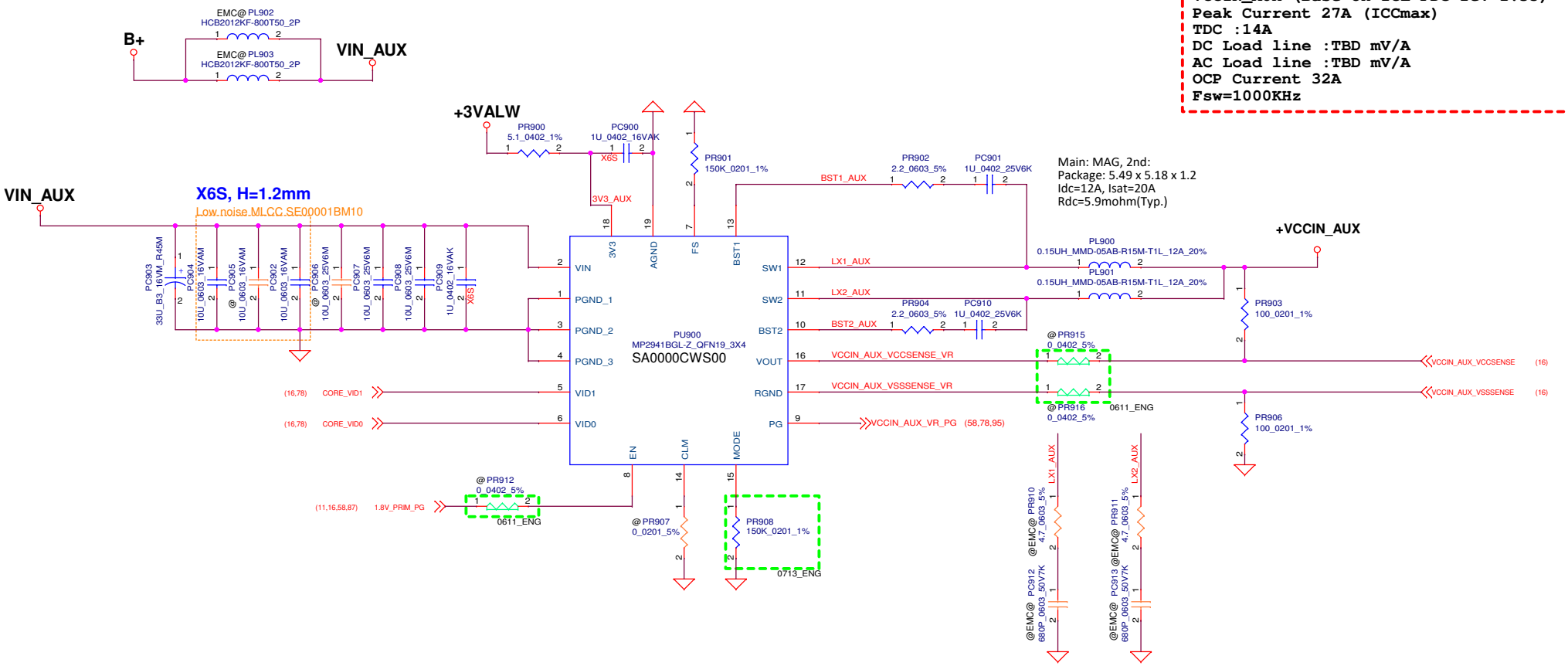

Table---1:VID control Bit logics

VID1	VID0	VOUT(V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

Table---2:CLM Select

State	CLM	Resistor to GND
M1	7A	0
M2	10A	90k
M3	13A	150k
M4	16A	>230k or float

Table---3:MODE Select

State	Interleaving	VID Down option	Resistor to GND
M1	N	Slew down	0
M2	Y	Slew down	90k
M3	Y	Decay	150k
M4	N	Decay	>230k or float

Table---4:FS Select

State	Fs(kHz)	Resistor to GND
M1	500	0
M2	700	90k
M3	1000	150k
M4	1200	>230k or float

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Title	PWR_VCCIN_AUX		
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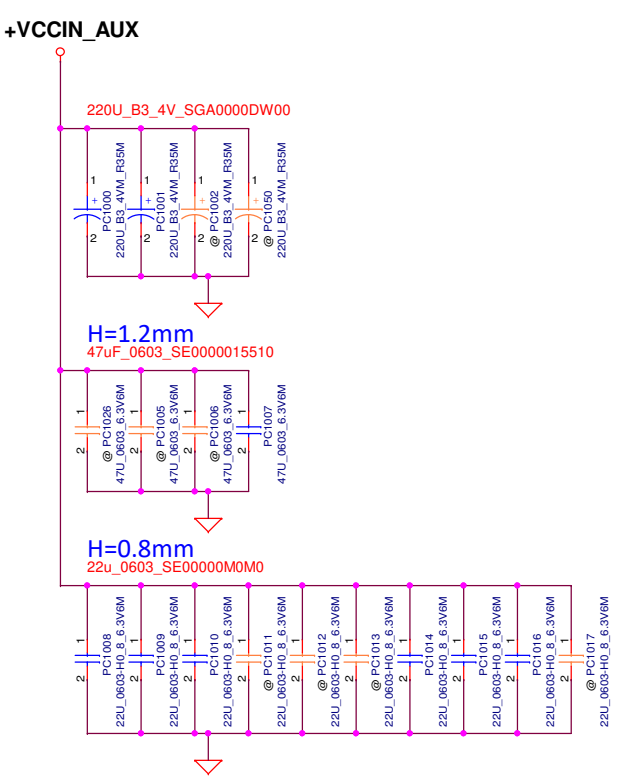
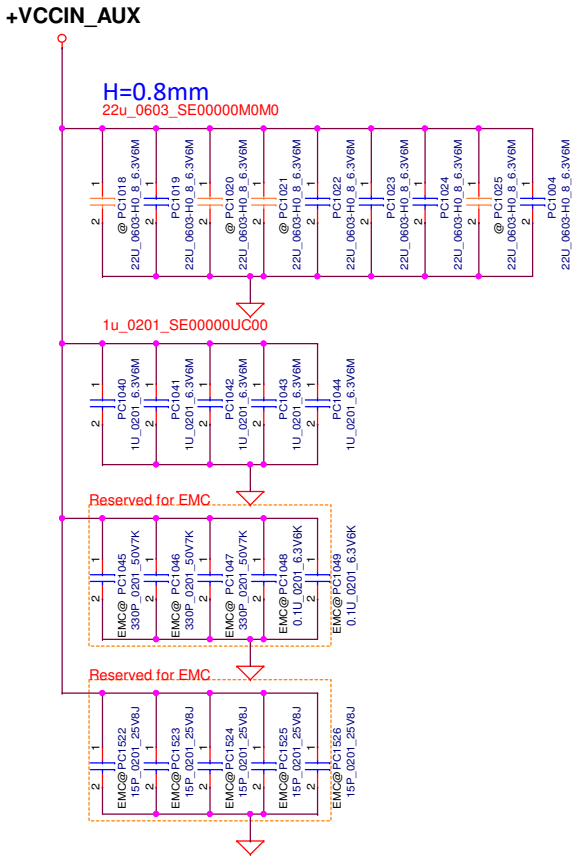
Support component(36.4)

PDG rev 0.5 for TGL U:
1x 220uF 7343
4x 47uF 0805
12x 22uF 0603
15x 10uF 0402

Compal: 2019/05/13
2x 220uF B3 (Reversed 2pcs)
1x 47uF 0603 (Reversed 3pcs)
11x 22uF 0603 (Reserved 8pcs)
5x 1uF 0201





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Compal Electronics, Inc.

Title: PWR_DECOUPLING-VCCIN_AUX

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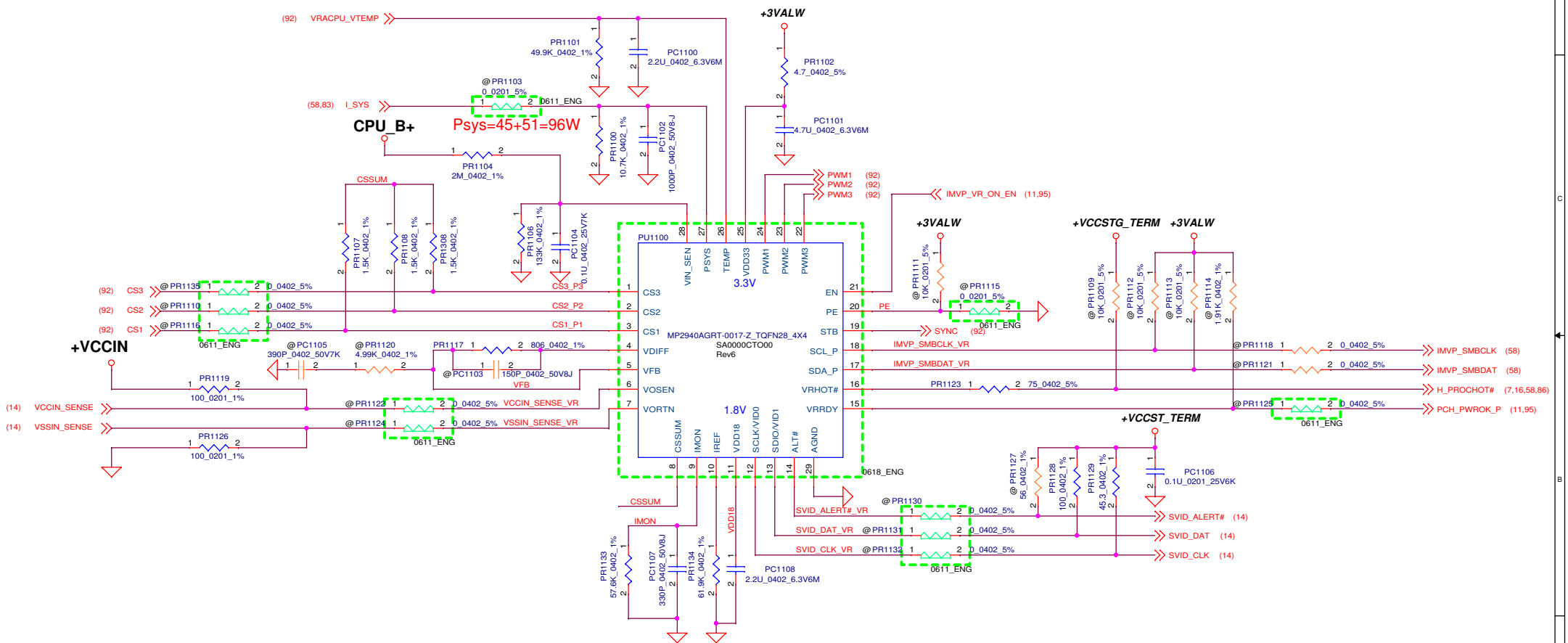
Controller(36.1), Support component(36.3)



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Compal Electronics, Inc.

Title: PWR_VCCIN_CTRL

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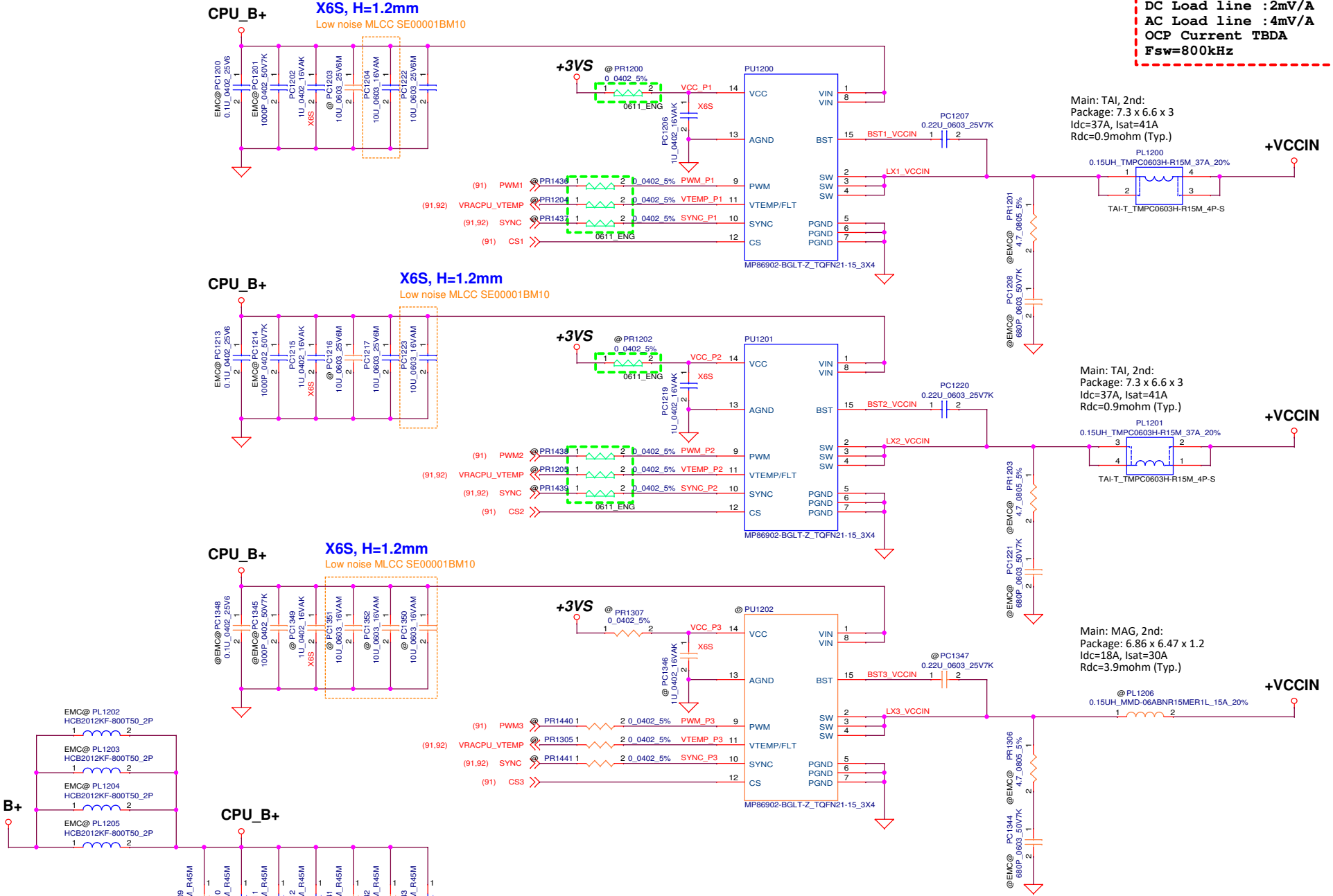
Support component(36.2),(36.3)

VCCIN (Base on ICL PDG rev 1.35)
Peak Current 55A (ICCmax)
PL2 TDC :36A
DC Load line :2mV/A
AC Load line :4mV/A
OCP Current TBDA
Fsw=800kHz



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Compal Electronics, Inc.

Title: PWR_VCCIN_Driver MOS

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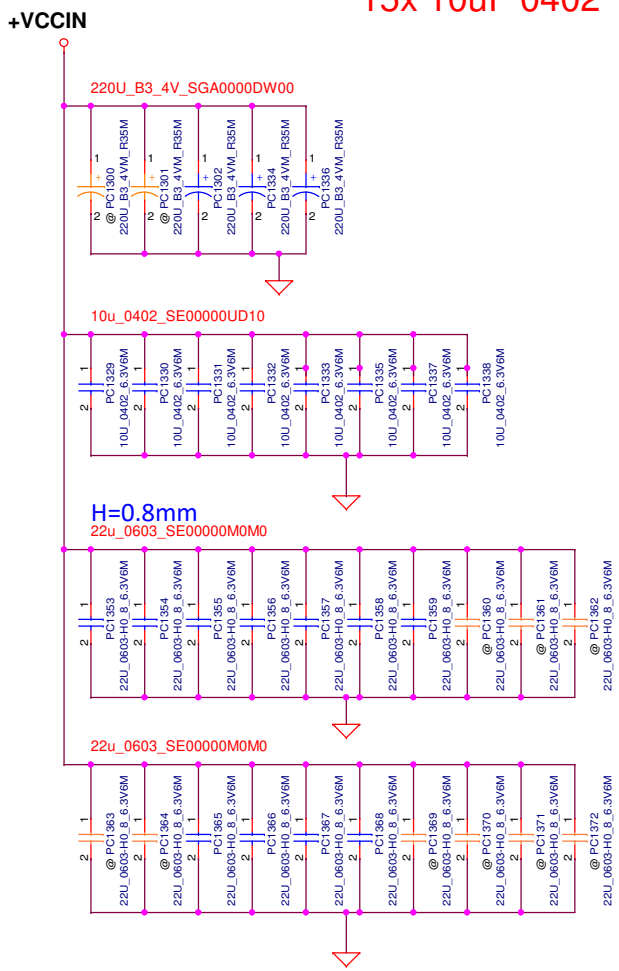
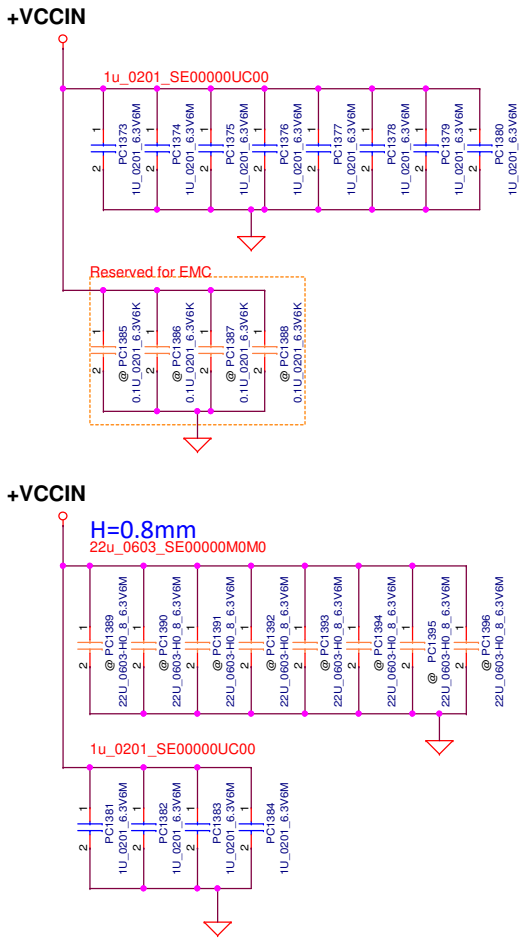
Support component(36.4)

PDG rev 0.5 for TGL U:
Primary side:
4x 220uF 7343
29x 10uF 0402
10x 22uF 0603
12x 1uF 0201
Backside:
15x 10uF 0402

Compal: 2019/05/13
3x 220uF B3 (Reserve 4pcs)
11x 22uF 0603 (Reserve 17pcs)
8x 10uF 0402
12x 1uF 0201





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Title	PWR_DECOUPLING-VCCIN		
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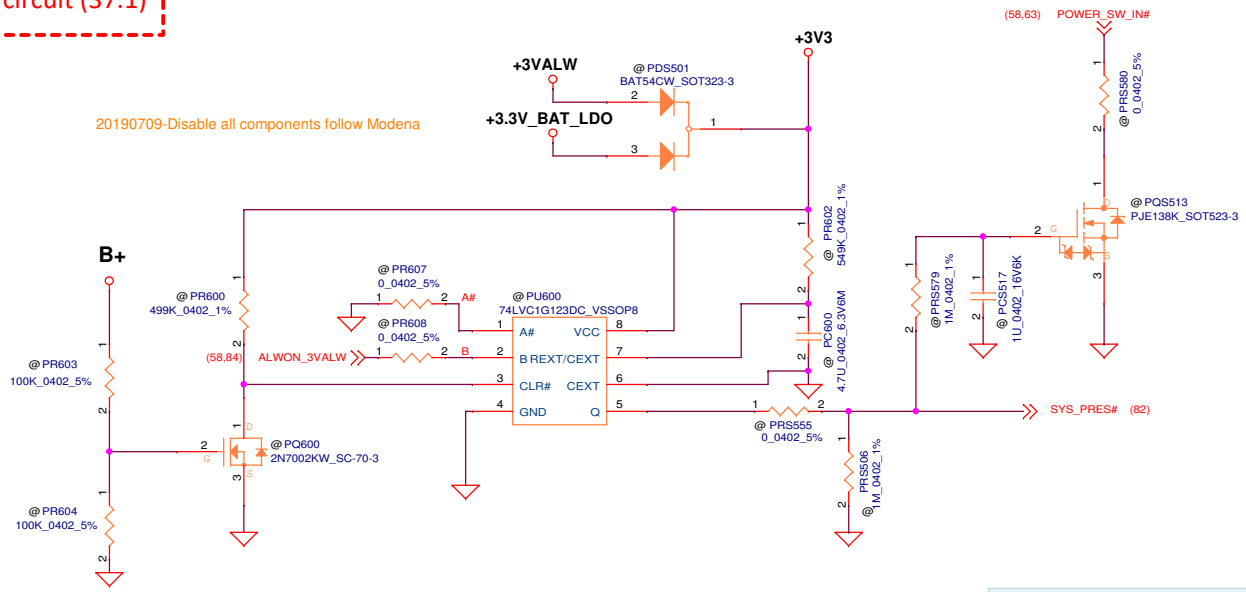
Storage mode wake up circuit (37.1)



Input			Output
CLR	$\overline{A}$	B	Q
L	X	X	L
X	H	X	L[2]
X	X	L	L[2]
H	L	↑	⎍
H	↓	H	⎍
↑	L	H	⎍

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Title: PWR_SHIP_MODE/ENBATN

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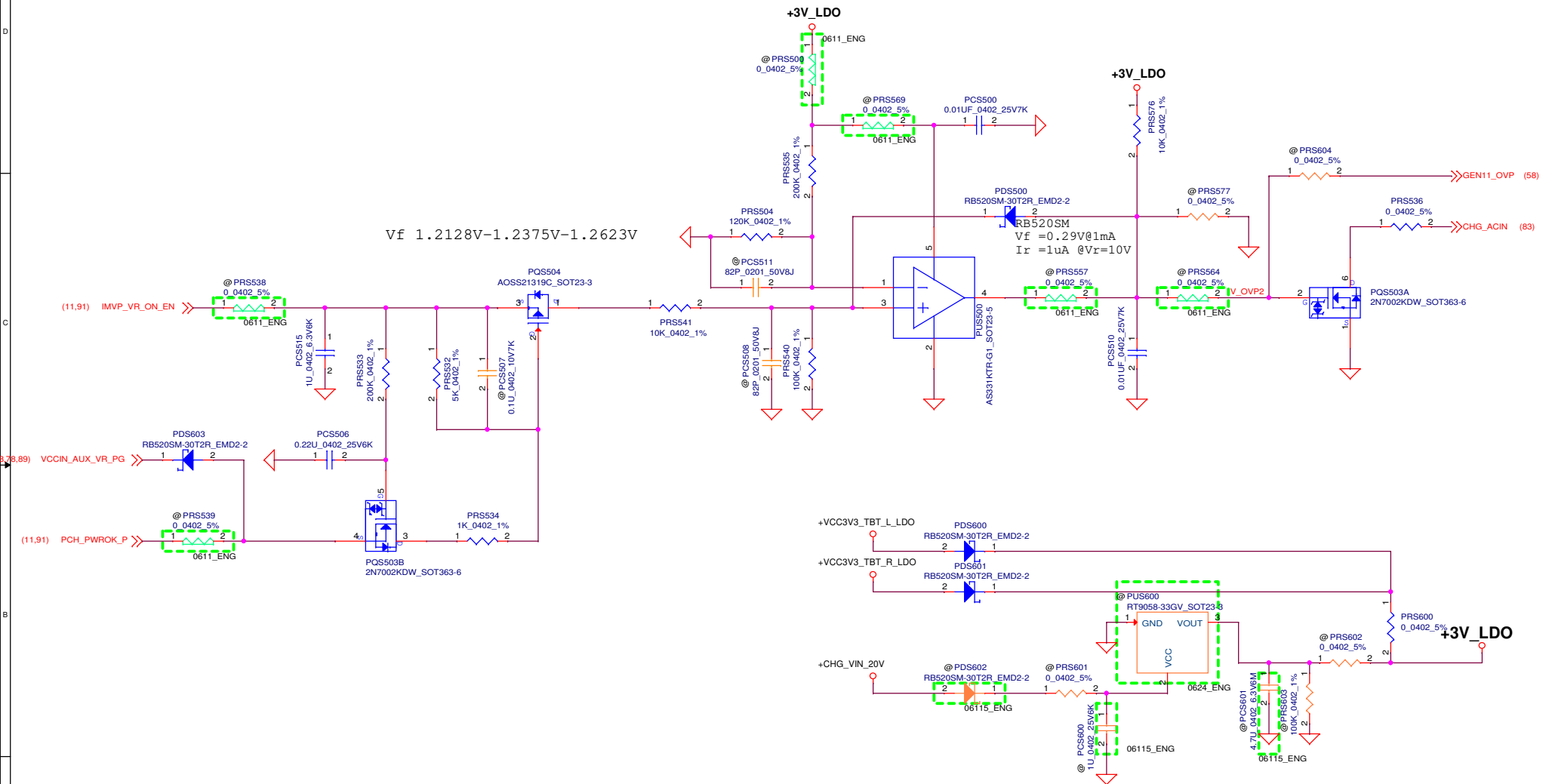
Vcore OVP (37.1)



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Title: RESERVE

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